Board of Studies
Master of Technology

(VLSI and Embedded Systems)

Revised Regulations, Curriculum and Syllabus
On Regulations 2018

(Non-CBCS)

(with effect from academic year 2021-2022)

Pondicherry University
Pondicherry - 605 014
INDIA

Table of Contents

Master of Technology

(VLSI and Embedded Systems)

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(Offered by Department of ECE of Sri Manakula Vinayagar Engineering College, Puducherry with effect from academic year 2021-2022)

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i) Revised Regulations for (Non – CBCS) M.Tech. (VLSI and Embedded Systems)

Besides the Non - CBCS regulations specified by Pondicherry University in respect of engineering post graduate degree admission, evaluation and awarding degree, the following norms are applicable for this programme.

1. Name of the Programme	M.Tech. (VLSI and Embedded Systems)
2. Nature of the Programme	Regular, Coming under Engineering Department.
3. Programme Duration	Two years (Four Semesters). However, one can complete the programme within maximum of eight semesters.
4. Eligibility Criteria	Candidates for admission to the first semester of four semester M.Tech (VLSI and Embedded Systems) should have passed B.E / B.Tech in Electronics and communication Engineering / Computer Science and Engineering/ Information Technology / Electrical and Electronics Engineering/ Instrumentation and Control Engineering/ Bio Medical Engineering/ Electronics and Instrumentation Engineering and other related branches, through regular course of study from an AICTE approved institution or an examination of any University or authority accepted by the Pondicherry University as equivalent thereto, with at least 55% marks in the degree examination or equivalent CGPA. Note: i. Candidates belonging to SC/ST who have a mere pass in the qualifying examination are eligible (as per university norms). ii. There is no age limit for M.Tech programmes.
5. Admission Criteria	The admission policy for various M.Tech programmes will be decided by the respective institutes offering M.Tech programmes subject to conforming to the relevant regulations of the Pondicherry University.
6. Intake	As per the sanctioned strength to the Institute by the Pondicherry University.
7. Teaching and Learning Methods	Lectures, tutorials and seminars are the main methods of course delivery, which would be supplemented by individual practical work, project work, simulation assignment, seminars and industrial visits.

8. Structure of M.Tech Programme

8.1 The M.Tech Programmes is of semester pattern with 16 weeks of instruction in a semester.

8.2 The programme of instruction for each stream of specialization will consist of:

i. Core courses (Compulsory)
ii. Electives
iii. Laboratory
iv. Online course
v. Internship
vi. Project work

8.3 Credits will be assigned to the courses based on the following general pattern:

i. One credit for each lecture period
ii. One credit for each tutorial period
iii. One credit for Project literature survey
iv. Two credits for practical course
v. Two credits for Online course
vi. Two credits for Internship
vii. Twelve credits for Project work
viii. One teaching period shall be of 60 minutes duration including 10 minutes for discussion and movement.

8.4 Regulations, curriculum and syllabus of the M.Tech programme shall have the approval of Board of Studies and other Boards /Committees / Councils, prescribed by the Pondicherry University. The curriculum should be so drawn up that the minimum number of credits and other requirements for the successful completion of the programme will be as given in Table 1.

Table 1: Curriculum Details of the Programme

S. No.	Description	Requirements M.Tech (Full-Time)
1	Number of Semesters	4
2	Min. No. of credits of the Programme	74
3	Max. No. of credits of the Programme	74
4	Min. Cumulative Grade Point Average for pass	5
5	Min. period of completion of the Programme (consecutive Semesters)	4
6	Max. period for completing the Programme (consecutive Semesters)	8
7	Number of core and elective courses	18
8	Online course	1
9	Laboratory	2
10	Project work (semesters)	2
11	Internship	1

8.5 A core course is a course that a student admitted to the M.Tech programme must successfully complete to receive the degree. A student must register for all the core courses listed in the curriculum.

	8.6 Elective courses are required to be chosen from the courses offered by the department(s) in that particular semester from among the approved courses. A core course of one department may be chosen as an elective by a student from other department[***]. [***]Note: A candidate should successfully complete 7 electives for the award of degree. However, it is mandatory that the electives for each semester should be from the group of electives listed in curriculum. 8.7 Project work is envisaged to train a student to analyze independently any problem posed to him/her. The work may be analytical, experimental, design or a combination of both. The project report is expected to exhibit clarity of thought and expression. 8.8 The medium of instruction, examination, seminar and project work will be in English.
9. Requirements to appear for University Examination	9.1 A candidate shall be permitted to appear for university examinations at the end of any semester only if he / she secures not less than 75% overall attendance arrived at by taking into account the total number of periods in all subjects put together offered by the institution for the semester under consideration. Candidates who secure overall attendance greater than 60% and less than 75% have to pay a condonation fee as prescribed by the University along with a medical certificate obtained from a medical officer not below the rank of Assistant Director to become eligible to appear for the examinations. 9.2 His / Her conduct should be satisfactory as certified by the Head of the institution.
10. Evaluation	10.1 Theory Courses: 40% of marks for internal and 60% for end semester examinations. The end semester question paper will have Part A ($6 \times 2 = 12$ Marks) consisting of six two mark questions and Part B ($4 \times 12 = 48$ Marks) consisting of six twelve mark descriptive questions of which one of them is compulsory and totally a candidate has to answer four out of six. For the end semester examination (University Semester Examination), the questions will be chosen only from the first four units of every theory subject of the programme to account end semester marks of 60 and internally (cumulatively) to assess a candidate's depth of knowledge in the concerned subject for 40 marks, a minimum of two internal tests (30 marks) shall be conducted. Further, the content of the fifth unit in each subject shall be considered to conduct seminars, tutorials, simulations, assignments, development of hardware models etc. for 10 marks as it is formulated at system level for all subjects of the programme. The question paper setter will be appointed by the Competent Authority of the University. However, the evaluation shall be a central evaluation that shall be carried out by Controller of Examinations, Pondicherry University. 10.2 Practical Courses: 50% of marks for internal and 50 % for the end semester examinations.

	10.3 Non-Class Room Course I: 100% of marks through internal assessment only. It is optional to undergo internship in established industry or esteemed institution / Seminar/ Workshop / Conference / FDP / Short term course / NPTEL/GIAN/MOOC Course for a period of four weeks (20 working days) either in single or multiple spans by a candidate. Further, a presentation should be given regarding the training or programme underwent during the period with the submission of a report. There shall not be any end semester evaluation. However, the internal evaluation is done by the committee comprising of internal members and one external member from other department of the same institute constituted by Head of the Department for the award of appropriate grade to the candidate based on the performance. The distribution of marks will be decided by the committee. The internship / Seminar/ Workshop / Conference / FDP / Short term course / NPTEL/GIAN/MOOC Course can be completed at any period of the duration of M.Tech. programme to fulfill the partial requirements for the award of M.Tech. degree. 10.4 Non-Class Room Course II: It is mandatory to undergo one course related to the chosen programme for the minimum period of 30 hours either from NPTEL or GIAN or MOOC that is to be completed at any period of the duration of M.Tech. programme to fulfill the partial requirements for the award of M.Tech. degree. Absolute grade shall be awarded to a candidate based on the marks given in the certificate issued by the competent authority (NPTEL or GIAN or MOOC) for the chosen course. 10.5 Project - Literature Survey: 100% of marks through internal assessment only. It is mandatory to undergo a complete literature survey by a candidate on the area of project work in the third semester regularly. There will be two reviews for the candidate on the literature survey carried out. There shall not be any end semester evaluation. However, the internal evaluation is based on the presentation of the candidate with the submission of a report about the literature survey. It will be done by the committee comprising of internal members and one external member from other department of the same institute constituted by Head of the Department for the award of appropriate grade to the candidate based on the performance. The distribution of marks for the literature survey will be decided by the committee. 10.6 Project and Viva Voce:50% of marks for internal and 50% for end semester examinations. The Project work shall be evaluated for a maximum of 100 marks. There shall be three assessments during the fourth semester by a review committee. The Head of the Department shall constitute the review committee consisting of supervisor, project coordinator and another faculty member from the Department for the internal assessment (30 marks). The contribution by the respective supervisor of a student for 20 marks shall be accounted for the internal marks of 50. The end semester Project Viva Voce (for 50

marks) shall be conducted by the external member nominated by the competent Authority of the University. The distribution of the marks is shown in the Table given below.

Table 2: Allocation of marks

Allocation of Marks for Project and Viva Voce (100 Marks)					
Internal (50 Marks)				**External (50 Marks)**	**Total (100 Marks)**
Review Committee (30 Marks)			Supervisor (20 Marks)		
First Review	Second Review	Third Review			
10 Marks	10 Marks	10 Marks	20 Marks	50 Marks	100 Marks

10.7 Publication: Mandatory requirement for the completion of the programme.

It is mandatory to have a minimum of one submitted manuscript / accepted publication in reputed journal during the M.Tech. programme. However, the submitted manuscript / accepted paper is subject to the recommendation of the evaluating committee comprising of internal members from same Department constituted by Head of the Department and one external member (examiner) from other institute nominated by competent Authority of University for the acceptance of the quality of the manuscript /paper of the candidate. The publication can be made at any period of the duration of M.Tech. programme. However, it does not contribute any credits to the programme but mandatory to fulfill the partial requirements for the award of M.Tech. degree. This evaluation process may be carried out along with even end semester examination depending up on the status of the students.

10.8 The end-semester examination shall be conducted by the Pondicherry University for all the courses offered by the department. A model question paper, as approved by the Chairperson, BOS (ECE), Pondicherry University, for each course offered under the curriculum should be submitted to the University.

10.9 The University shall adopt the double valuation procedure for evaluating the end-semester examinations, grading and publication of the results. Each answer script shall be evaluated by two experts. If the difference between the total marks awarded by the two examiners is not more than 15% of end-semester examination maximum marks, then the average of the total marks awarded by the two examiners will be reckoned as the mark secured by the candidate; otherwise, a third examiner is to be invited to evaluate the answer scripts and his/her assessment shall be declared final.

10.10 Continuous assessment of students for theory courses shall be based on two tests (15 marks each) and one assignment (10 marks). A laboratory course carries an internal assessment mark of 50 distributed as follows: (i) Regular laboratory exercises and records – 20 marks (ii) Internal laboratory test– 20 marks and (iii) Internal viva-voce – 10 marks.

10.11 All eligible students shall appear for the University examination.

11. Grading

11.1 The assessment of a course will be done on absolute marks basis. However, for the purpose of reporting the performance of a candidate, letter grades, each carrying stipulated points, will be awarded as per the range of total marks (out of 100) obtained by the candidate, as detailed below in Table 3.

Table 3: Letter Grade and the Corresponding Grade Point

Range of Total Marks	Letter Grade	Grade Point	Description
90 to 100	S	10	Excellent
80 to 89	A	9	Very Good
70 to 79	B	8	Good
60 to 69	C	7	Above Average
55 to 59	D	6	Average
50 to 54	E	5	Satisfactory
0 to 49	F	0	Failure
-	FA	-	Failure due to lack of attendance
-	AB	-	Failure by absence

11.2 A student is deemed to have completed a course successfully and earned the appropriate credit if and only if, he /she receives a grade of E or above. The student should obtain 40% of marks in the University examination in a subject to earn a successful grade.
A candidate shall be declared to have passed the examination in a subject of study only if he/she secures not less than 50% of the total marks (Internal assessment plus university examination marks).

11.3 A candidate who has been declared "Failed" in a course may reappear for that subject during the subsequent semester and secure a pass.

11.4 The internal assessment marks secured by a student in a theory course shall be considered only during the first appearance. For the subsequent attempts, the marks secured by the student in the University examination shall be scaled up to the total marks. Further, the marks secured by the student in the University examination in the latest attempt shall alone remain valid in total suppression of the University examination marks secured by the student in earlier attempts.

12. Declaration of Results, Rank and Issue of Grade Card	12.1 The results will be declared and the grade cards will be issued to the students after completing the valuation process. 12.2 The grade cards will contain the following details: i. The college in which the candidate is studying/has studied. ii. The list of courses enrolled during the semester and the grades scored. iii. The Grade Point Average (GPA) for the semester and the Cumulative Grade Point Average (CGPA) of all enrolled subjects from first semester onwards. 12.3 GPA is the ratio of the sum of the products of the number of Credits (C) of courses registered and the corresponding Grade Point (GP) scored in those courses, taken for all the courses and the sum of number of credits of all the courses GPA = (Sum of (C × GP)/ Sum of C) The sum will cover all the courses the student has taken in that semester, including those in which he/she has secured F. 12.4 CGPA will be calculated in a similar manner, considering all the courses enrolled from first semester. FA grades are to be excluded for calculating GPA and CGPA. If a student has passed in a course after failing in earlier attempts, the grade secured by the student in the successful attempt only will be taken into account for computing CGPA. 12.5 To convert CGPA into percentage marks, the following formula shall be used: % Mark = (CGPA - 0.5) × 10 12.6 A candidate who satisfies the course requirements for all semesters and passes all the examinations prescribed for all the four semesters within a maximum period of eight (8) semesters reckoned from the commencement of the first semester to which the candidate was admitted, shall be declared to have qualified for the award of degree. 12.7 A candidate who qualifies for the award of the degree shall be declared to have passed the examination in FIRST CLASS with DISTINCTION upon fulfilling the following requirements: i. Should have passed all the subjects pertaining to semesters 1 to 4 in his/her first appearance in 4 consecutive semesters starting from first semester to which the candidate was admitted. ii. Should not have been prevented from writing examinations due to lack of attendance. iii. Should have secured a CGPA of 8.50 and above from semesters 1 to 4. 12.8 A candidate who qualifies for the award of the degree by passing all the subjects relating to semesters 1 to 4 and secure CGPA not less than 6.5 shall be declared to have passed the examination in FIRST CLASS. All other candidates who qualify for

	the award of degree shall be declared to have passed the examination in SECOND CLASS. 12.9 A student with CGPA less than 5.0 is not eligible for the award of degree. 12.10 For the award of University rank and gold medal, the CGPA secured from 1st to 4th semester should be considered and it is mandatory that the candidate should have passed all the subjects from 1st to 4th semester in the first appearance and he/she should not have been prevented from writing the examination due to lack of attendance and should not have withdrawn from writing the University examinations.
13. Provision for Withdrawal	A candidate may, for valid reasons, and on the recommendation of the Head of the Institution be granted permission by the University to withdraw from writing the entire semester examination as one UNIT. The withdrawal application shall be valid only if it is made earlier than the commencement of the last theory examination pertaining to that semester. Withdrawal shall be permitted only once during the entire programme. Other conditions being satisfactory, candidates who withdraw are also eligible to be awarded DISTINCTION whereas they are not eligible to be awarded a rank/gold medal.
14. Temporary Discontinuation from the Programme	If a candidate wishes to temporarily discontinue the programme for valid reasons, he/she shall apply through the Head of the Institution in advance and obtain a written order from the University permitting discontinuance. A candidate after temporary discontinuance may rejoin the programme only at the commencement of the semester at which he/she discontinued, provided he/she pays the prescribed fees to the University. The total period of completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not in any case exceed 4 years, including the period of discontinuance.
15. Revision of Regulations and Curriculum	The University may from time to time revise, amend or change the regulations of curriculum and syllabus as and when requirement for the same arises.
16. Power to Modify	15.1 Notwithstanding anything contained in the foregoing, the Pondicherry University shall have the power to issue directions/ orders to remove any difficulty. 15.2 Nothing in the foregoing may be construed as limiting the power of the Pondicherry University to amend, modify or repeal any or all of the above.
17. Minimum number of credits to be acquired for successful completion of the programme	74 (Seventy Four) Credits

ii) Revised Curriculum of M.Tech. (VLSI and Embedded Systems)

I Semester

Sl. No.	Course Code	Name of the Course	H/S	L-T-P	Credits
1	VEENG 510	VLSI Design Laboratory	H	0-0-4	2
2	VEENG 511	Applied Mathematics	H	3-1-0	4
3	VEENG 512	Digital System Design	H	3-1-0	4
4	VEENG 513	Microcontroller Based System Design	H	3-1-0	4
5	VEENG 514	VLSI Design Techniques	H	3-1-0	4
6		Elective I	S	2-1-0	3
7		Elective II	S	2-1-0	3
				Total Credits for Semester I	**24**

(H – Hard Core Course; S – Soft Core Course)

II Semester

Sl. No.	Course Code	Name of the Course	H/S	L-T-P	Credits
8	VEENG 520	Embedded System Design Laboratory	H	0-0-4	2
9	VEENG 521	Advanced Digital System Design	H	3-1-0	4
10	VEENG 522	Embedded Networking	H	3-1-0	4
11	VEENG 523	Embedded System Design	H	3-1-0	4
12	VEENG 524	Low Power Digital VLSI Design	H	3-1-0	4
13		Elective III	S	2-1-0	3
14		Elective IV	S	2-1-0	3
				Total Credits for Semester II	**24**

(H – Hard Core Course; S – Soft Core Course)

III Semester

Sl. No.	Course Code	Name of the Course	H/S	L-T-P	Credits
15.		Elective V	S	2-1-0	3
16.		Elective VI	S	2-1-0	3
17.		Elective VII	S	2-1-0	3
18.	VEENG 610	Non-Class Room Course I	H	0-0-2	2
19.	VEENG 611	Non-Class Room Course II	H	0-2-0	2
20.	VEENG 612	Project – Literature Survey	H	0-0-1	1
				Total Credits for Semester III	**14**

(H – Hard Core Course; S – Soft Core Course)

IV Semester

Sl. No.	Course Code	Name of the Course	H/S	L-T-P	Credits
21.	VEENG 620	Project and Viva Voce	H	0-0-12	12
22.	VEENG 621	Publication	-	-	0
				Total Credits for Semester IV	**12**

(H – Hard Core Course; S – Soft Core Course)

Total number of credits required to complete M.Tech in VLSI and Embedded Systems : 74 credits

Semester I – List of Electives

Sl. No.	Course Code	Name of the Course	L-T-P	Credits
1.	VEENG 530	Embedded Technology	2-1-0	3
2.	VEENG 531	FPGA based System Design	2-1-0	3
3.	VEENG 532	Modeling and Synthesis with Verilog HDL	2-1-0	3
4.	VEENG 533	Physical Design of VLSI	2-1-0	3
5.	VEENG 534	Real Time Operating System	2-1-0	3
6.	VEENG 535	Soft Computing	2-1-0	3
7.	VEENG 536	Software for Embedded System	2-1-0	3
8.	VEENG 537	VLSI Architecture	2-1-0	3

Semester II - List of Electives

Sl. No.	Course Code	Name of the Course	L-T-P	Credits
1.	VEENG 550	DSP Processor Architecture and Programming	2-1-0	3
2.	VEENG 551	Embedded Control System	2-1-0	3
3.	VEENG 552	High Speed Digital Design	2-1-0	3
4.	VEENG 553	Principles of ASIC Design	2-1-0	3
5.	VEENG 554	Real Time Systems	2-1-0	3
6.	VEENG 555	RISC Processor Architecture and Programming	2-1-0	3
7.	VEENG 556	Testing of VLSI Circuits	2-1-0	3
8.	VEENG 557	VLSI Signal Processing	2-1-0	3

Semester III - List of Electives

Sl. No.	Course Code	Name of the Course	L-T-P	Credits
1.	VEENG 630	Advanced Embedded System	2-1-0	3
2.	VEENG 631	Advanced Image Processing	2-1-0	3
3.	VEENG 632	CAD for VLSI Circuits	2-1-0	3
4.	VEENG 633	Design of Analog and Mixed VLSI Circuits	2-1-0	3
5.	VEENG 634	Distributed Embedded Computing	2-1-0	3
6.	VEENG 635	Hardware Software Co-Design	2-1-0	3
7.	VEENG 636	Micro-Electromechanical Systems	2-1-0	3
8.	VEENG 637	Nano Electronics	2-1-0	3
9.	VEENG 638	Pervasive Devices and Technology	2-1-0	3
10.	VEENG 639	Robotics and Automation	2-1-0	3
11.	VEENG 640	System-on-Chip Design	2-1-0	3
12.	VEENG 641	VLSI for Wireless Communication	2-1-0	3

iii) Syllabus for M.Tech. (VLSI and Embedded Systems) :

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 510	VLSI DESIGN LAB	0	0	4	2	60

Objective : Hands on experience on various simulation tools to design and analyze the combinational and sequential circuits.

LIST OF EXPERIMENTS:
(Given the list is minimal, however, the course teacher can decide the level of experiments)

1. Design and simulate combi national circuits using VHDL/Verilog HDL in Gate level , behavior level and generate test vectors
   a. Adder, subtractor circuits
   b. Code converter circuits
   c. Decoder circuit
   d. Encoder circuit
   e. Multiplexer
   f. Demultiplexer
   g. Parallel adder/subtractor
   h. Multiplier
   i. Divider
2. Design and simulate sequential circuits using VHDL/Verilog HDL in Gate level , behavior level and generate test vectors
   a. Flip-flops
   b. Shift registers (SISO, SIPO,PISO,PIPO)
   c. Synchronous counter
   d. Asynchronous counter
   e. Mod counter
   f. Sequence generator
   g. Sequence detector
   h. Ring and Johnson counter
3. Simulation of NMOS and CMOS circuits using SPICE.
4. FPGA/CPLD real time programming and I/O interfacing.
5. Implementation of combinational circuit in FPGA/CPLD
6. Implementation of sequential circuit in FPGA/CPLD

VEENG 510

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 511	APPLIED MATHEMATICS	3	1	0	4	60

Prerequisite: Knowledge in Graph theory and Boolean functions.

Objective : To learn the Boolean functions, Graphical and Optimization techniques in the design and analysis of systems.

Outcome : The students will understand the different concepts of Graphs, Boolean algebra and Operation Research and will be able to solve problems in the engineering field.

Unit I: Basics of Graph Theory **12 Hours**

Graphs : Data structures for graphs - Subgraphs - Operations on Graphs Connectivity - Euler, Hamilton graph and its properties - Planar graphs; Networks and the maximum flow - Minimum cut theorem - Trees : Spanning trees - Rooted trees - Matrix representation of graphs.

Unit II : Graph Algorithm **12 Hours**

Computer Representation of graphs: Basic graph algorithms - Minimal spanning tree algorithm - Kruskal and Prim's algorithm - Shortest path algorithms - Dijsktra's algorithm - DFS and BFS algorithms; Lattices as partially ordered sets: properties of Lattices. Lattices as Algebraic Systems- Sublattices

Unit III: Boolean Algebra **12 Hours**

Definitions and examples: Subalgebra - Direct Product and Homomorphism-Boolean Functions- Representation and Minimization of Boolean Functions- Design examples using Boolean Algebra.

Unit IV: Optimization Techniques **12 Hours**

Linear Programming: Formulation of LPP - Graphical methods - Simplex method- Transportation problems- Assignment problems.

Unit V: Instructional Activities **12 Hours**

Applications of Boolean Functions - Practical applications of Basic graph algorithms, Transportation problems and Assignment problems.

Reference Books:

1. Tremblley J P and Manohar R, Discrete Mathematics Structures with Application to Computer Science, Mc Graw Hill Book Company, 2017
2. Narsingh Deo, Graph Theory: With Application to Engineering and Computer Science, PHI, 2014.
3. Kanti Swarup, Man Mohan and P. K. Gupta, Operations Research, Sultan Chand & Sons, 2014.
4. Rao S S, Engineering Optimization: Theory and Practice, New Age International Pvt. Ltd., 3rd Edition 2018.

Hyperlinks:

1. http:// www.nptel.ac.in

VEENG 511

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 512	DIGITAL SYSTEM DESIGN	3	1	0	4	60

Prerequisite: Basics of Electronics and Programming

Objective : To expose the students in the fundamentals of combinational and sequential circuits and study the concepts of VHDL for digital circuits

Outcome : Design and analyze combinational and sequential circuits using VHDL code

Unit I: Digital Systems Overview **12 Hours**

Review of combinational circuits: Adder - subtractor - code converter- decode-, encoder- Multiplexer- demultiplexer.;Review of sequential circuits: Flip-flops- shift registers-synchronous counter- ripple counter- mod counter- ring counter-Johnson counter- non sequential counters.

Unit II: Hardware Description Language **12 Hours**

VHDL Description of Combinational Networks: Modelling Flip-flops using VHDL Processes-VHDL Models for a Multiplexer-Compilation and Simulation of VHDL Code ; Modelling a Sequential Machine : Variables - Signals- and Constants- Arrays VHDL Operators-VHDL Functions- VHDL Procedures - Packages and Libraries.

Unit III: Design of Networks for Arithmetic Operations **12 Hours**

Design of Parallel adder/subtractor with accumulator : Serial adder with accumulator- design of binary multiplier and binary divider- signed multiplier using VHDL.

Unit IV: Designing with Programmable Logic Devices **12 Hours**

Read Only Memories: Programmable Array Logic PALs- Programmable Logic Arrays PLAs - PLA minimization and PLA folding; Other Sequential PLDs- Design of combinational circuits using PLD's.

Unit V: Instructional Activities **12 Hours**

Simulation of logic gates- adder- subtractor- decoder-multiplexer-flip flops- counters using VHDL.

Reference Books:

1. Charles H. Roth, Fundamentals of Digital Design, Jr., PWS Pub. Co., 7th Edition, 2014.
2. Kenneth J Breeding, Digital Design Fundamentals, Prentice Hall, Englewood Cliffs, New Jersey.1989.
3. William I. Fletcher, A Systematic Approach to Digital Design, PHI, 1996.
4. Charles H. Roth, Digital System Design using VHDL, Thomson Learning, 3rd Edition, 2007.
5. James E. Palmer, David E. Perlman, Introduction to Digital Design, Tata McGraw Hill, 1996.
6. Devadas A. Ghosh and K. Keutzer, Logic Synthesis, McGraw Hill, 1994.
7. N. N Biswas, Logic Design Theory, 1st Edition, Prentice Hall of India, 1993.
8. John F. Wakerly, Digital Design Principles and Practices, Prentice Hall, 4th Edition, 2001.

Hyperlinks:

1. http://www2.cs.uidaho.edu/~krings/CS449
2. http://www.cs.colostate.edu/~malaiya/530/08/1Intro.pdf
3. http://www.ida.liu.se/~TDDB47/lectures/tddb47-dependability-2x3.pdf

VEENG 512

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 513	MICROCONTROLLER BASED SYSTEM DESIGN	3	1	0	4	60

Prerequisite : Knowledge in Digital Electronics, Architecture and programming in Microprocessors

Objective : To impart knowledge on Microcontroller based system design and its application

Outcome : Able to understand and analyze the Microcontroller Architecture and peripherals with its application

Unit I : 8051 Architecture **12 Hours**

Architecture: Memory organization - Addressing modes - Instruction set -Timers - Interrupts - I/O ports, Interfacing I/O Devices - Serial Communication.

Unit II : Programming **12 Hours**

Assembly language programming : Arithmetic Instructions - Logical Instructions -Single bit Instructions - Timer Counter Programming - Serial Communication Programming Interrupt Programming ; RTOS for 8051 : RTOS Lite - Full RTOS - Task creation and run - LCD digital Clock/thermometer using Full RTOS

Unit III : PIC Microcontroller **12 Hours**

Architecture : Memory organization - Addressing modes - Instruction set - PIC programming in Assembly & C - I/O port- Data Conversion - RAM & ROM Allocation - Timer programming,

Unit IV : Peripheral of PIC Microcontroller **12 Hours**

Timers: Interrupts - I/O ports - I2C bus - A/D converter - UART- CCP modules -ADC, DAC and Sensor Interfacing - Flash and EEPROM memories.

Unit V: Instructional Activities **12 Hours**

Microcontroller based system design: Interfacing LCD Display - Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control - Controlling DC/ AC appliances - Measurement of frequency - Stand alone Data Acquisition System.

Reference Books:

1. Muhammad Ali Mazidi, Janice G. Mazidi and Rolin D. McKinlay, The 8051 Microcontroller and Embedded Systems, Prentice Hall, 2005.
2. Muhammad Ali Mazidi, Rolin D. Mckinlay and Danny Causey, PIC Microcontroller and Embedded Systems using Assembly and C for PIC18', Pearson Education 2008
3. John Iovine, PIC Microcontroller Project Book, McGraw Hill 2000
4. Myke Predko, Programming and Customizing the 8051 Microcontroller, Tata McGraw Hill2001.
5. Rajkamal, Microcontrollers-Architecture, Programming, Interfacing & System design, 2nd Edition, Pearson Education, 2012.
6. I Scott Mackenzie and Raphael C.W. Phan, The Micro controller, Pearson Education, 4th Edition 2012

Hyperlinks:

1. http:// www.nptel.iitm.ac.in
2. http:// www.microchip.com/design-centers/microcontrollers
3. https://learn.mikroe.com/

VEENG 513

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 514	VLSI DESIGN TECHNIQUES	3	1	0	4	60

Prerequisite : Basic concepts in Digital Circuit Design

Objective : To understand the design and analysis of digital VLSI chips using CMOS technology

Outcome : Can understand the design issues at the layout, transistor logic and register-transfer level.

Unit I : MOS transistor theory and process technology **12 hours**

NMOS and PMOS transistors: Threshold voltage - Body effect- Design equations - Second order effects. MOS models and small signal AC characteristics- Basic CMOS technology.

Unit II : Inverters and Logic gates **12 hours**

NMOS and CMOS Inverters: Stick diagram- Inverter ratio- DC and transient characteristics - switching times- Super buffers- Driving large capacitance loads; CMOS logic structures: Transmission gates- Static CMOS design- Dynamic CMOS design.

Unit III : Circuit characterization and Performance estimation **12 hours**

Resistance estimation - Capacitance estimation – Inductance - switching characteristics- transistor sizing - power dissipation and design margining. Charge sharing .Scaling.

Unit IV : VLSI system components, circuits and design **12 hours**

Multiplexers - Decoders – comparators - priority encoders - Shift registers - Arithmetic circuits: Ripple carry adders- Carry look ahead adders- High-speed adders; Multipliers. Physical design - Delay modeling - cross talk - floor planning - power distribution - Clock distribution; Basics of CMOS testing.

Unit V: Instructional Activities **12 Hours**

Case study on Overview of digital design with Verilog HDL for Structural - Data flow - Behavioral Styles of Hardware Description

.

Reference Books:

1. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd Edition, 2000.
2. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley &Sons, Inc., 2002.
3. Samir Palnitkar, Verilog HDL, Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
5. J. Bhasker and B. S.Publications, A Verilog HDL Primer, 2nd Edition, 2001.
6. Pucknell, Basic VLSI Design, Prentice Hall of India Publication, 1995.
7. Wayne Wolf, Modern VLSI Design System on Chip, Pearson Education, 2002.

Hyperlinks:

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in.

VEENG 514

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 520	EMBEDDED SYSTEM DESIGN LABORATORY	0	0	4	2	60

Objective : Hands on experience to design various applications for microcontroller based system design in order to acquire sufficient knowledge and to understand embedded system design based applications.

LIST OF EXPERIMENTS:
(Given the list is minimal, however, the course teacher can decide the level of experiments)

1. Interfacing the microcontroller to a PC through RS232 and displaying the messages sent by the microcontroller on the PC.

2. Design With PIC and Arduino Microcontrollers - Assembly or C Programming/Arduino IDE programming to interface
   a. 7 segment displays to display the measured voltage from 0 to 5 volts
   b. LDR to display light intensity in 7 segment display
   c. Temperature sensor to display temperature in 7 segment display
   d. Pressure sensor to display measured pressure in 7 segment display
   e. PH sensor to display measured value in 7 segment display
   f. Ultrasonic sensor to display distance in 7 segment display
   g. Noise sensor to display noise level in 7 segment display

3. Interface DC motor with Microcontroller and control its speed and direction using PWM

4. Microcontroller based system design
   a. Lamp controller using a light sensor and a timer
   b. Water Pump Controller to maintain water level in a tank
   c. Moisture controller using moisture and sprinkler controller

5. Design Real time clock

6. Wireless data transfer using Microcontroller

7. Color identification and tracking using Raspberry pi

VEENG 520

Course Code	Name of the Course	Periods			Credits	Total Hours
VEENG 521	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	4	60
		3	1	0		

Prerequisite : Knowledge on digital integrated circuit design, Verilog and FPGA.

Objective : To make the students to understand the design and analysis of the synchronous and asynchronous sequential circuits.

Outcome : The students will be able to design sequential circuits and fault diagnosis algorithms.

Unit I: Sequential Circuit Design **12 Hours**

Analysis of clocked synchronous sequential circuits and modeling: state diagram - state table - state table assignment and reduction - design of iterative circuits - ASM chart and realization using ASM.

Unit II: Asynchronous Sequential Circuit Design **12 Hours**

Analysis of asynchronous sequential circuit: Design of asynchronous sequential circuit - static and dynamic methods - flow table reduction - races - state assignment transition table and problems in transition table - essential hazards - data synchronizers - mixed operating mode asynchronous circuits.

Unit III: Synchronous Design Using Programmable Devices **12 Hours**

Programming logic device families: Designing a synchronous sequential circuit using PLA/PAL - realization of finite state machine using PLD/FPGA.

Unit IV: Fault Diagnosis And Testability Algorithms **12 Hours**

Fault diagnosis method: Path sensitization method - Boolean difference method - D – algorithm - tolerance techniques - compact algorithm - fault in PLA/PAL- test generation - built in self test.

Unit V: Instructional Activities **12 Hours**

Simulation of synchronous/ asynchronous sequential circuits: Logic compilation - two level and multi level logic synthesis - sequential logic synthesis -technology mapping - tools for mapping to PLDs and FPGAs.

Reference books:

1. Charles H R Jr and Larry L K, Fundamentals of Logic Design, 7th Edition, Global Engineering, 2004.
2. Nripendra N B, Logic Design Theory, Prentice Hall of India, 1993.
3. Parag K L, Fault Tolerant and Fault Testable Hardware Design, 1st Edition, B S Publications, 2002.
4. Parag K L, Digital System Design using PLD, B S Publications,1990
5. Charles H R Jr, Digital System Design using VHDL, 2nd Edition, CL Engineering, 2007
6. Michael D C, Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL, Prentice Hall, 1999.

Hyperlinks:

1. https://www.um.edu.mt/data/assets/pdf_file/0016/120625/adsd.pdf
2. http://nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf
3. https://www.doulos.com/knowhow/verilog_designers_guide/
4. https://www.nandland.com/

VEENG 521

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 522	EMBEDDED NETWORKING	3	1	0	4	60

Prerequisite : Basic knowledge in Microcontrollers

Objective : To impart knowledge on communication protocols, USB and CAN bus Embedded Ethernet

Outcome : Design and development of Serial and parallel communication, USB and CAN bus for Embedded networking

Unit I : Embedded Communication Protocols **12 hours**

Embedded Networking: Introduction - Serial/Parallel Communication - Serial communication protocols - RS232 standard - RS485 - Synchronous Serial Protocols -Serial Peripheral Interface (SPI) - Inter Integrated Circuits (I^2 C) - PC Parallel port programming -ISA/PCI Bus protocols - Fire wire

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Unit II : USB and CAN bus **12 hours**

USB bus: Introduction - Speed Identification on the bus - USB States - USB bus communication: Packets - Data flow types - Enumeration –Descriptors- PIC-18 Microcontroller USB Interface - C Programs - CAN Bus : Introduction - Frames -Bit stuffing -Types of errors -Nominal Bit Timing - PIC microcontroller CAN Interface -A simple application with CAN.

Unit III : Ethernet Basics **12 hours**

Elements of a network: Inside Ethernet - Building a Network: Hardware options - Cables, Connections and network speed - Design choices: Selecting components -Ethernet Controllers - Using the internet in local and internet communications - Inside the Internet protocol. Gigabit Ethernet.

Unit IV: Embedded Ethernet **12 hours**

Exchanging messages using UDP and TCP - Serving web pages with Dynamic Data - Serving web pages that respond to user Input - Email for Embedded Systems - Using FTP - Keeping Devices and Network secure.

Unit V: Instructional Activities **12 Hours**

Serial and parallel protocols used in industries – its timing diagram, Serial communication with an Arduino, visualize the Ethernet traffic using protocol analyzer.

.

Reference Books:

1. Frank Vahid and Givargis, Embedded Systems Design: A Unified Hardware/Software Introduction, Wiley Publications, 2012.
2. Jan Axelson, Parallel Port Complete, Penram Publications, 2005.
3. Dogan Ibrahim, Advanced PIC Microcontroller Projects in C, Elsevier, 2008.
4. Jan Axelson, Embedded Ethernet and Internet Complete, Penram Publishing (India) Pvt. Ltd., 2003.
5. Bhaskar Krishnamachari, Networking Wireless Sensors, Cambridge Press, 2005.
6. Gerard Hartnett and Peter Barry, Designing Embedded Network Applications, Intel Press, 2005.

Hyperlink:

1. http:// www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu
3. http://web.iiit.ac.in/~bezawada/CN.html

VEENG 522

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 523	EMBEDDED SYSTEM DESIGN	3	1	0	4	60

Prerequisite : Basic Knowledge in Digital Electronics and microcontroller

Objective : To understand basic concepts, Building Blocks for Embedded System development

Outcome : Design real time embedded systems using the concepts of RTOS and ability to understand the role of embedded systems in industry

Unit I: Introduction **12 Hours**

Embedded system overview, Design challenge: Optimizing design metrics- Processor Technology- General purpose Processors- Single purpose Processors and Application Specific Processors; IC Technology: Full custom/VLSI, Semicustom ASIC- PLD- Trends- Design Technology

Unit II : Custom Single purpose Processor **12 hours**

RTL combinational components: RTL sequential components - Custom Single purpose Processor Design- RTL Custom Single purpose Processor Design- Optimizing Custom Single purpose Processors- Optimizing the original program- Optimizing the FSMD- Optimizing the data path- optimizing the FSM

Unit III : General purpose Processors **12 hours**

Basic architecture: Data path- Control Unit - Memory - Instruction execution and Pipelining; Superscalar and VLIW architectures- Application Specific Instruction set Processors (ASIP's), Microcontrollers- DSP- Less General ASIP environments- Selecting a Microprocessor and General purpose processor design.

Unit IV : Embedded OS **12 hours**

Creating embedded operating system: Basis of a simple embedded OS - Introduction to sEOS - Using Timer 0 and Timer 1- Portability issue-Alternative system architecture- Important design considerations when using sEOS.

Unit V: Instructional Activities **12 Hours**

Study of Digital Camera - Example-User's perspective, Designer's perspective, Requirements, Specification, Informal functional specification, Nonfunctional specification, Executable specification. Design and Implementation of 8051 based design, Implementation of Fixed point FDCT, Implementation of Hardware FDCT.

Reference Books:

1. Frank Vahid and Tony Givargis, Embedded System Design A Unified Hardware/Software Introduction, John Wiley & Sons, 2014.
2. Steve Heath Embedded System Design, Butterworth Heinemann, 2010.
3. Gajski and Vahid, Specification and Design of Embedded Systems, Prentice Hall, 1994.
4. C.M. Krishna and Kang G. Shin, Real Time Systems, The McGraw Hill International Editions Computer Science Series, 1997.
5. Rajkamal, Embedded System, Tata McGraw Hill, 2003.
6. Charls Roth, Digital System Design using VHDL, Tata McGraw Hill, 2007.
7. Rettberg A, Zanella M, Domer R, Gerstlauer A and Rammig F, Embedded System Design: Topics, Techniques and Trends, Springer, 2007.

Hyperlinks:

1. http:// www.nptel.ac.in/courses/117106030/35
2. http://link.springer.com
3. http://www.ee.iitm.ac/videolecturesl

VEENG 523

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 524	LOW POWER DIGITAL VLSI DESIGN	3	1	0	4	60

Prerequisite : Fundamentals of VLSI design.

Objective : To discuss low power design methodologies at various design levels from the circuit level to the system level and also power estimation with optimization techniques.

Outcome : Students will be able to design low power VLSI circuits.

Unit I: Power Dissipation **12 hours**

Introduction: Need for low power circuit design - sources of power consumption -design methodology - low power figure of merits - limits and applications of low power VLSI Design

Unit II: Power Analysis **12 hours**

Power Analysis: SPICE circuit simulation - discrete transistor modeling and analysis - gate level 0 logic simulation - architecture level analysis - data correlation analysis; Probabilistic Power Analysis: Random logic signals - probabilistic power analysis techniques - signal entropy.

Unit III: Circuit and Logic Level **12 hours**

Circuit Level: Transistor and gate sizing - equivalent pin ordering - network restructuring and reorganization - special latches and flip flops; Logic Level: Gate reorganization - signal gating - logic encoding - precipitation logic.

Unit IV: Energy Recovery Techniques **12 hours**

Energy Recovery Techniques: Energy dissipation using the RC model - energy recovery circuit design - power reduction in clock networks - low power bus - delay balancing.

Unit V: Instructional Activities **12 Hours**

Simulation Study: Sources of power dissipation in SRAMs - Low power SRAM circuit techniques; Sources of power dissipation in DRAMs - Low power DRAM circuit techniques using related tools

Reference Books:

1. Kaushik R and Sharat C P, Low-Power CMOS VLSI Circuit Design, Wiley Student Edition, 2009.
2. Gary K Y, Practical Low Power Digital VLSI Design, Kluwer Academic Publishers, 1998.
3. Bellaouar A and Elmasry M, Low-Power Digital VLSI Design: Circuits and Systems, Kluwer Academic Publishers, 1995.
4. Chandrakasan A and Robert W B, Low-Power CMOS Design, Wiley-IEEE Press, 1998.
5. Rabaey J M and Massoud P, Low Power Design Methodologies, Kluwer Academic Publishers, 1995.
6. Kiat-Seng Y and Kaushik R, Low-Voltage, Low-Power VLSI Subsystems, Tata McGraw Hill Professional Engineering, 2009.
7. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002.

Hyperlinks:

1. http://www.nptel.iitm.ac.in/courses/106105034/
2. http://www.eeherald.com/section/design-guide/Low-Power-VLSI-Design.html

VEENG 524

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 530	EMBEDDED TECHNOLOGY	2	1	0	3	45

Prerequisite : Basic Knowledge in communication networks

Objective : To study the basics of OSI reference model and introduce multiboard communication software.

Outcome : Understand the concept of switches and routers for protocol implementation and design the communication protocol for multiboard

Unit I: OSI Reference Model **9 Hours**

Communication Devices – Communication Echo System – Design Consideration – Host Based Communication – Embedded Communication System – OS Vs RTOS.

Unit II: Software Partitioning **9 Hours**

Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Layer2 Switch – Layer3 Switch / Routers – Protocol Implementation – Management Types – Debugging Protocols.

Unit III: Tables & Other Data Structures **9 Hours**

Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

Unit IV: Management Software **9 Hours**

Device Management – Management Schemes – Router Management – Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

Unit V: Instructional Activities **9 Hours**

Implementation of 7 layer OSI in CIM: A case study, Connecting a classified network to the Internet – Embedded Communication System- An internet Routing and firewall security. Simulation of Partitioning of Structures, Simulation of Speeding Up access.

Reference Books:

1. Sridhar T, Designing Embedded Communication Software, CMP Books, 2003.
2. Comer D, Computer networks and Internet, Sixth Edition, 2016
3. Larry L Peterson, Computer Networks: A Systems Approach, Morgan Kaufmann, 2007.
4. Edward Insam, TCP/IP Embedded Internet Applications, Newness, 2003.
5. Bruce Powel Douglas, Design Patterns for Embedded Systems in C, Newness, 2011.
6. Daneil W. Lewis, Fundamentals of Embedded Software, Prentice Hall 2004.
7. Malcom G. Lane, Data communication Software Design, BOYD & Fraser Publication, 1985.

Hyperlinks:

1. https://www.crcpress.com/Designing-Embedded-Communications-Software
2. ieeexplore.ieee.org/abstract/document/6976507
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com
5. https://sans.org

VEENG 530

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 531	FPGA BASED SYSTEM DESIGN	2	1	0	3	45

Prerequisite: Knowledge on Digital system design and fundamentals of PLD

Objective : To provide in depth understanding of logic and system design, synthesis of advanced digital hardware systems in FPGA tools

Outcome : Design and model the digital circuits with HDL at behavioral, structural, and RTL Levels and implemented in FPGA

Unit I: FPGA Architecture **9 Hours**

Introduction of basic concepts: Digital design and FPGAs- FPGA based system design- Logic blocks- Routing architecture- FPGA Fabrics- Circuit design of FPGA fabrics- Platform FPGA.

Unit II: Technology mapping for FPGAs **9 Hours**

Fundamental of high level synthesis: Logic synthesis- Logic optimization and technology mapping - Lookup table technology mapping- Timing analysis- Timing optimization- Area optimization.

Unit III: Routing for FPGAs **9 Hours**

Routing terminology - Strategy for routing in FPGAs -Routing for row-logic block selection- Experimental procedure Logic block architecture -Logic block functionality vs area and efficiency- Logic block selection- Experimental procedure-Logic block area and routing model.

Unit IV: Architecture of FPGAs **9 Hours**

Study of Xilinx Virtex series FPGAs, Architecture of Altera cyclone FPGA series. Comparison of Xilinx & Altera FPGAs

Unit V: Instructional Activities **9 Hours**

Synthesis of multiplier and digital filters in FPGA- Analyse the FPGA architecture and mapping of I/O pads

Reference Books:

1. Wayne Wolf, FPGA based System Design, Prentice Hall, 2004.
2. Wayne Wolf, Modern VLSI Design, System on Chip Design, 3rd Edition, Prentice Hall, 2002.
3. S. Trimberger and Edr, Field Programmable Gate Array Technology, Kluwer Academic Publication, 2009.
4. Ian Kuon, Russell Tessier and Jonathan Rose, FPGA Architecture, Now Publishers, 2008.
5. Rajeev Murgai, Robert King Brayton and Al Berto, Logic Synthesis for FPGAs, Kluwer Academic Publishers, 1993.
6. P. K. Chan and S. Mourad, Digital Design using Field Programmable Gate Arrays, Prentice Hall, 1994.
7. John Voldfield and Richard C Dore, Field Programmable Gate Arrays, Wiley, 1995.

Hyperlinks:

1. http://nptel.iitm.ac.in

VEENG 531

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 532	MODELLING AND SYNTHESIS WITH VERILOG HDL	2	1	0	3	45

Prerequisite : Basic Knowledge in Digital Circuits And Hardware Modeling

Objective : To introduce the concepts of hardware modeling with Verilog HDL, synthesis of logic circuit and also study the electronic design automation in VLSI.

Outcome : Exposure in layout/design and design automation process.

Unit - I : Hardware Modeling With Verilog HDL **9 Hours**

HDLs in EDA: System C, VHDL and Verilog- System Verilog overview- Hardware Encapsulation- Hardware Modeling with Verilog HDL- Hierarchical descriptions of hardware- Structured design methodology- Arrays, Using Verilog for synthesis- Event driven simulation and test benches- Logic system, data types and operators; User-defined primitives: Combinational behavior-Sequential behavior.

Unit - II: Delay Models, Behavioral Description **9 Hours**

Verilog models of propagation delay: Built-in constructs- Inertial delay,- Time scales and precision- Delays- Delay effects and Pulse rejection- Race condition in Verilog- Types of race condition- Task and function- Events, Process control, Disable a block- Watchdog- debugging, Code coverage- Testing strategies- File handling- Behavioral descriptions in Verilog HDL

Unit - III: Synthesis of Combinational Logic, Sequential Logic **9 Hours**

Synthesis of Combinational Logic: HDL-Based Synthesis, Technology-Independent Design, Synthesis Methodology- Styles for Synthesis of Combinational Logic- Technology Mapping and Shared Resources- Three-State Buffers- Outputs and Don't Cares, Synthesis of Sequential Logic,Latches- Edge-Triggered Flip-Flops, Registered Combinational Logic- Shift Registers and Counters

Unit - IV: Synthesis of Language Constructs, Switch Level Models **9 Hours**

Synthesis of Language constructs: MOS Transistor Technology- Switch-Level Models- PULL gates- CMOS Transmission gates- Bi-Directional gates (Switches) - Signal Strengths- Strength Reduction by Primitives- Combination and Resolution of Signal Strengths- Signal Strengths and Wired Logic

Unit- V: Instructional Activities **9 Hours**

Case Studies on VLSI Design Automation tools-An overview of the features of practical CAD tools – Modelsim - Leonardo spectrum -Xilinx ISE - Quartus II - VLSI backend tools –IC Station, Cadence and Synopsis.

References Books:

1. M, D, Ciletti, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 2006.
2. Steven M. Rubin, Computer Aids for VLSI Design, http://www.rulabinsky.com/cavd (free online book), 1997.
3. M. G. Arnold, Verilog Digital – Computer Design, Prentice Hall, 2006.
4. S. Palnitkar, Verilog HDL – A Guide to Digital Design and Synthesis, Pearson, 2003.
5. M. J. S. Smith, Application Specific Integrated Circuits, Pearson Education, 2008.
6. M. H. Rashid, Spice for Circuits and Electronics using PSPICE, PHI 1995.
7. S-Edit v13.0 user guide by Tanner EDA tool.

Hyperlinks:

1. http://web.ewu.edu
2. http://nptel.iitm.ac.in

VEENG 532

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 533	PHYSICAL DESIGN OF VLSI	2	1	0	3	45

Prerequisite: Basic concepts in digital circuit design

Objective : To introduce the physical design concepts such as routing, placement, partitioning and packaging

Outcome : The students will be able to understand the design concepts and circuit layouts

Unit I: Introduction To VLSI Technology **9 Hours**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein-Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

Unit II: Placement Using Top-Down Approach **9 Hours**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut-partition with capacity and i/o constraints; Floor planning: Rectangular dual floor planning-hierarchical approach- simulated annealing- Floor plan sizing; Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement

Unit III: Routing Using Top Down Approach **9 Hours**

Fundamentals: Maze running- line searching- Steiner trees; Global Routing: Sequential Approaches- hierarchical approaches- multi-commodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming; Detailed Routing: Channel Routing-Switch box routing; Routing in FPGA: Array based FPGA- Row based FPGAs

Unit IV: Performance Issues In Circuit Layout **9 Hours**

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization

Unit V: Instructional Activities **9 Hours**

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over the Cell (OTC) Routing- Multiple chip modules (MCM) - Programmable Logic Arrays- Transistor chaining-Wein-Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction

Reference Books:

1. Sarafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1995.
2. Preas M. Lorenzatti, Physical Design and Automation of VLSI Systems, Benjamin Cummins Publishers, 1998.
3. Ban Wong et.al, Nano CMOS Circuit and Physical Design, Wiley 2004.
4. N. A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic, 2002.
5. Sadiq M. Sait and Habib Youssef, VLSI Physical Design Automation, Theory and Practice, World Scientific Publishing Company, 2003.
6. Bryan T. Preas, Physical Design Automation of VLSI System, Benjamin Cummins Publishers, 1998.
7. Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2010.

Hyperlink:

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in

VEENG 533

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 534	REAL TIME OPERATING SYSTEM	2	1	0	3	45

Prerequisite : Basic knowledge in Computer Programming and microcontroller based system

Objective **:** To expose the fundamentals of interaction of OS with a computer and application development using RTOS

Outcome **:** Acquire knowledge in the basic concept of embedded system

Unit I: Structure Of RTOS µCOS / Embedded Linux **9 Hours**

RTOS features- Resources and shared resources Task, Task control block- Task scheduling-Task level context switching- Syntax related to Context switching- Locking and unlocking of scheduler- Idle & Static task- Interrupt under RTOS- ISR under RTOS - Servicing an interrupt- Clock Tick. Initialization and Starting the RTOS- Multitasking- Task Management function- Event Control Blocks-Task State Management.

Unit II: Synchronization & Communication in µCOS-II / Embedded Linux **9 Hours**

Semaphore management Functions with µCOS-II / Embedded Linux API - ECB as Semaphore, Mutual exclusion Semaphore functions- Event Flag management Functions- Mailbox management- ECB As Mailbox- Message Queue management- ECB as Message Queue- Message Queue Management Function

Unit III: Process, I/O, Memory Management in RTOS **9 Hours**

Process Management- Timer functions- Device- File- I/O subsytems management- Memory Management- Memory Control Block- Dynamic memory allocation.

Unit IV: WinCE **9 Hours**

Introduction : WinCE- Polled Loop Systems – RTOS Porting to a Target, Explanation of Application- Kernel- OAL- Explanation of CPU- SOC, Platform- MMU; MMU for ARM based devices in WinCE- Overview of Boot loader- eboot Directory Structure, Implementing Startup Code- Comparison study of µCos-II- Embedded Linux- Real Time Linux- Vx-Works- QNX Nutrino- ThreadEX.

Unit V: Instructional Activities **9 Hours**

Design and simulate static and dynamic scheduling algorithms in suitable platform- Study of RTOS used for Washing Machine- Air Conditioner- Microwave Oven- Engine Management System using CAN- Automatic Chocolate Vending Machine

Reference Books:

1. Silberschatz, Galvin and Gagne, Operating System Concepts, 6th Edition, John Wiley, 2003.
2. D. M. Dhamdhere, Operating Systems, A Concept-Based Approch, Tata McGraw Hill, 2008.
3. Dreamtech Software Team, Programming for Embedded Systems, Wiley Publishing Inc., 2003.
4. Jean J. Labrosse, Micro C/OS-II The Real Time System Kernel, 2nd Edition, CPM Books, 2002.
5. K. V. K. K Prasad, Embedded/Real Time Systems: Concepts, Design and Programming – The Ultimate Reference, Dreamtech Press, 2003.
6. Sriram Iyer and Pankaj Gupta, Embedded Real Time Systems Programming, Tata McGraw Hill Publishing Company Limited, 2004.
7. David E. Simon, An Embedded Software Primer, Pearson Education Asia, First Indian Reprint 2000.
8. Samuel Phuns, Professional Windows Embedded CE 6.0, Wrox, 2008.
9. Rajkamal, Embedded System, Tata McGraw Hill, 2003.

Hyperlinks:

1. http:// www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu
3. http://web.iiit.ac.in/~bezawada/CN.html

VEENG 534

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 535	SOFT COMPUTING	2	1	0	3	45

Prerequisite : Fundamentals of VLSI design.

Objective : To discuss low power design methodologies at various design levels from the circuit level to the system level and also power estimation with optimization techniques.

Outcome : Students will be able to design low power VLSI circuits.

Unit I: Neural Network **9 Hours**

Basic concept - mathematical model - properties of neural networks - architectures - different learning methods - common activation functions - application of neural networks; Neuron architecture: Algorithms - McCullo h-Pitts - Back propagation NN - ADALINE - MADALINE - Discrete Hopfield net - BAM - Maxnet.

Unit II: Fuzzy Sets & Logic **9 Hours**

Fuzzy versus Crisp - fuzzy sets - fuzzy relations - laws of propositional logic - inference - Predicate logic fuzzy logic - quantifiers - inference - defuzzification methods.

Unit III: Genetic Algorithm **9 Hours**

Role of GA - fitness function - selection of initial population - cross over (different types) - mutation - inversion - deletion - constraints handling and applications of travelling salesman and graph coloring.

Unit IV: Hybrid Systems **9 Hours**

Hybrid Systems: GA based BPNN (Weight determination) - Neuro fuzzy systems - Fuzzy BPNN - fuzzy neuron - architecture - learning - Fuzzy logic controlled genetic algorithm.

Unit V: Instructional Activities **9 Hours**

Simulation of PSD - HSA and ACO related to either wireless networking or Antenna or Image Processing using related tools.

References Books:

1. S. N. Sivanandam and S. N. Deepa, Principles of Soft Computing, 2nd Edition, John Wiley India, 2012.
2. S. Haykin, Neural Networks - A Comprehensive Foundation, 2nd Edition, Pearson Education, 2005.
3. T. S. Rajasekaran and G. A. VijaylakshmiPai, Neural Networks, Fuzzy Logic & Genetic Algorithms – Synthesis and Applications, Prentice-Hall India, 2003.
4. Sanchez, Takanori and Zadeh, Genetic Algorithm and Fuzzy Logic System, World Scientific, 1997.
5. Goldberg David, Genetic Algorithms, Pearson Education, 2006.
6. Zimmermann H J, Fuzzy Set Theory & Its Applications, Allied Publishers Ltd., 1991.
7. Stamatios V. Kartolopoulos Understanding Neural Networks and Fuzzy Logic: Basic Wiley-IEEE Press, 1995.

Hyperlinks:

1. https://www.tutorialspoint.com/biometrics/pattern_recognition_and_biometrics.htm
2. http://www.cedar.buffalo.edu/~srihari/CSE555/
3. https://www.ibm.com/developerworks/library/cc-beginner-guide-machine-learning-ai-cognitive/index.html

VEENG 535

Course Code	Name of the Course	Periods			Credits	Total Hours
VEENG 536	SOFTWARE FOR EMBEDDED SYSTEMS	L	T	P	3	45
		2	1	0		

Prerequisite : Basic Programming knowledge in C.

Objective : To introduce embedded software development process and Web enabling of systems.

Outcome : Gain knowledge and understanding of fundamental embedded systems design paradigms, architectures, possibilities and challenges, both with respect to software and hardware.

Unit I: Programming Embedded Systems **9 Hours**

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

Unit II: Python **9 Hours**

Overview of Embedded C - Compilers and Optimization - Programming and Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

Unit III: Embedded Program And Software Development Process **9 Hours**

Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java- Software Development process: Analysis – Design- Implementation – Testing – Validation- Debugging - Software maintenance.

Unit IV: Unified Modeling Language **9 Hours**

Object State Behaviour – UML State charts – Role of Scenarios in the Definition of Behavior – Timing Diagrams – Sequence Diagrams – Event Hierarchies – Types and Strategies of Operations – Architectural Design in UML Concurrency Design – Representing Tasks – System Task Diagram – Concurrent State Diagrams – Threads. Mechanistic Design – Simple Patterns.

Unit V: Instructional Activities **9 Hours**

Implement a state machine in embedded C to control RGB LED- Implement CAN bus Protocol-Testing sensors: Soil Moisture sensor-Web security - Case study: Web-based Home Automation system.

Reference Books:

1. David E. Simon, An Embedded Software Primer, Pearson Education, 2003.
2. Michael Barr, Programming Embedded Systems in C and C++, Oreilly, 2003.
3. H. M. Deitel, P. J. Deitel and A. B. Golldberg, Internet and World Wide Web – How to Program, 3rd Edition, Pearson Education, 2001.
4. Bruce Powel Douglas, Real-Time UML: Developing Efficient Object for Embedded Systems, 2nd Edition, Pearson Education, 2002.
5. Daniel W. Lewis, Fundamentals of Embedded Software where C and Assembly Meet, PHI 2002.
6. Raj Kamal, Embedded Systems - Architecture, Programming and Design, Tata McGraw Hill, 2006.
7. Jean J. Labrosse, Jack Ganssle, Robert Oshana, Colin Walls, Keith E. Curtis, Jason Andrews, David J. Katz, Rick Gentile, Kamal Hyder and Bob Perrin, Embedded Software, Newness, 2007.

Hyperlinks:

1. https://www.zapmeta.ws
2. http://nptel.ac.in/courses/117106030/35
3. https://link.springer.com
4. https://www.theengineeringprojects.com

VEENG 536

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 537	VLSI ARCHITECTURE	2	1	0	3	45

Prerequisite : Basic knowledge in logic circuit design

Objective : To introduce the features, programming and applications of programmable logic devices. Provide VLSI system design experience using FSM

Outcome : Students will be able to make the system level designs using FSM and analyze the performance with FPGA.

Unit I: CMOS Design **9 Hours**

Overview of digital VLSI design Methodologies- Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- Layout diagram, Stick diagram-IC fabrications – Trends in IC technology.

Unit II: Programmable Logic Devices **9 Hours**

Programming Techniques-Anti fuse-SRAM-EPROM and EEPROM technology – Re Programmable Devices Architecture-Function blocks, I/O blocks, Interconnects, XilinxXC9500,Cool Runner - XC-4000,XC5200, SPARTAN, Virtex - Altera MAX 7000-Flex 10KStratix.

Unit III: Basic Construction, Floor Planning, Placement And Routing **9 Hours**

System partition – FPGA partitioning – Partitioning methods- floor planning – placement physical design flow – global routing – detailed routing – special routing- circuit extraction – DRC.

Unit IV: Analog VLSI Design **9 Hours**

Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Speed and High frequency op-amps-Super MOS-Analog primitive cells-realization of neural networks.

Unit V: Instructional Activities **9 Hours**

Synthesis of the Ripple Carry Adder, Multiplier, Comparator, Shift registers and ALU circuits in CPLD devices and analyze the design with architecture.

Reference Books:

1. M. J. S Smith, Application Specific Integrated Circuits, Addition Wesley Longman Inc.1997.
2. Kamran Eshraghian, Douglas A. Pucknell and Sholeh Eshraghian, Essentials of VLSI Circuits and System, Prentice Hall, India, 2005.
3. Wayne Wolf, Modern VLSI Design, Prentice Hall, India, 2006.
4. Mohamed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, McGraw Hill International Editions, 1994.
5. Samir Palnitkar, Veri Log HDL, A Design Guide to Digital and Synthesis, 2nd Editions, Pearson, 2005.
6. John P. Uyemera Chip Design for Ssubmicron VLSI CMOS Layout and Simulation, Cengage Learning India Edition, 2011.

Hyperlinks:

1. http://courses.engr.wisc.edu/ece/ece755.html
2. http://www.ul.ie/graduateschool/course/vlsi-systems-meng.html
3. http://web.engr.oregonstate.edu/~sllu/ece474.html
4. http://www.vlsisystemdesign.com.html

VEENG 537

Course Code	Name of the Course	Periods			Credits	Total Hours
VEENG 550	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	3	45
		2	1	0		

Prerequisite : Basic Knowledge in processors, filter design and programming

Objective : To understand the techniques involved in real time DSP system and to design and implement a variety of algorithms for real world applications.

Outcome : Get familiar with the DSP processor architectures and practical knowledge with real time application.

Unit I: Digital Signal Processing Systems **9 Hours**

Introduction to Digital signal processor architectures: Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

Unit II: Digital Signal Processors **9 Hours**

TMS320C62x AND TMS320C64x: Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Real time implementations.

Unit III: Implementation of Fast Fourier Transforms **9 Hours**

Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

Unit IV: FIR and IIR Filter Implementations **9 Hours**

FIR and IIR filters: Characteristics – Structures - FIR Filter design using Windowing and frequency sampling method - IIR Filter-Butterworth and Chebyshev Filter Design- Fixed point implementation using TMS320C64x - Floating point implementation using TMS320C67x.

Unit V: Instructional Activities **9 Hours**

Simulate Auto Correlation and Cross correlation - Linear and circular Convolution- DFT/FFT, Design of FIR filter- Design of IIR filter

Reference Books:

1. B. Venkata Ramani and M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, TMH, 2004.
2. John G Proakis and Manolakis, Digital Signal Processing Principles, Algorithms and Applications, Pearson, 4th Edition, 2007.
3. Lapsley et al., DSP Processor Fundamentals, Architectures and Features, S. Chand & Co., 2000, Reprint.
4. Sen M. Kuo and Woon-Seng S. Gan, Digital Signal Processors – Architectures, Implementations and Applications, Pearson Education, 2005, Second Impression, 2009.
5. A. V. Oppenheim, R. W. Schafer and J. R. Buck, Discrete Time Signal Processing, Pearson, 2004.
6. S. K. Mitra, Digital Signal Processing, A Computer Based approach, Tata McGraw-Hill, 1998.

Hyperlinks:

1. http://www.nptel.iitm.ac.in/courses
2. https://link.springer.com

VEENG 550

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 551	EMBEDDED CONTROL SYSTEM	2	1	0	3	45

Prerequisite : Basic Knowledge in Micro controller

Objective : To expose the students to the fundamentals of Embedded System Blocks, fundamental RTOS and the Applications development

Outcome : Can understand and Design the embedded software for specific application

Unit I: Embedded System Organization **9 Hours**

Embedded computing – characteristics of embedded computing applications – embedded system design challenges; Build process of Real time Embedded system – Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit –ISA, EISA bus;

Unit II: Real-Time Operating System **9 Hours**

Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output – Non maskable interrupt, Software interrupt; Thread – Single, Multithread concept; Multitasking Semaphores.

Unit III: Interface With Communication Protocol **9 Hours**

Design methodologies and tools – design flows – designing hardware and software Interface. – system integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming;

Unit IV: Design Of Software For Embedded Control **9 Hours**

Software abstraction using Mealy-Moore FSM controller- Layered software development,-Basic concepts of developing device driver – SCI – Software - interfacing & porting using standard C & C++ ; Functional and performance Debugging with benchmarking Real-time system software

Unit V: Instructional Activities **9 Hours**

Interface A/D & D/A converter- Design of Digital voltmeter- Interface PWM motor and control its speed, serial communication interface.

References Books:

1. Steven F. Barrett and Daniel J. Pack, Embedded Systems – Design and Applications with the 68HC 12 and HCS12, Pearson Education, 2008.
2. Raj Kamal, Embedded Systems - Architecture, Programming and Design, Tata McGraw Hill, 2006.
3. Micheal Khevi, The M68HC11 Microcontroller Application in Control, Instrumentation and Communication, PH NewJersy, 1997.
4. Chattopadhyay, Embedded System Design, PHI Learning, 2011.
5. Muhammad Ali Mazidi, Rolin D. Mckinlay and Danny Causey, PIC Microcontroller and Embedded Systems - Using Assembly and C for PIC18, Pearson Education, 2008.
6. Steven F. Barrett and Daniel J. Pack, Embedded Systems - Design and Application with the 68HC12 & HCS12, Pearson Education, 2008.
7. Daniel W. Lewis, Fundamentals of Embedded Software, Prentice Hall, India, 2004.
8. Jack R Smith, Programming the PIC Microcontroller with MBasic, Elsevier, 2007.
9. Keneth J. Ayala, The 8086 Microprocessor: Programming and Interfacing the PC, Thomson India Edition, 2009.

Hyperlinks:

1. www.programmingembedded system.com
2. https://en.wikibooks.org/wiki/Embedded_Control_Systems_Design
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com

VEENG 551

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 552	HIGH SPEED DIGITAL DESIGN	2	1	0	3	45

Prerequisite : Basic knowledge in digital system design and electronics

Objective : To identify sources affecting the speed of digital circuits and to improve the signal transmission characteristics

Outcome : Ability to identify sources affecting the speed of digital circuits and to improve the signal transmission characteristics.

Unit I: Introduction **9 Hours**

Frequency, time and distance - Capacitance and Inductance Effects - High speed properties of logical gates - Speed and power modeling of wires - Geometry and Electrical properties of wires - Electrical model of Transmission lines - Lossless LC transmission lines - Lossy RLC transmission lines - Special transmission lines.

Unit II: Power Distribution and Noise **9 Hours**

Power supply network - Local power regulation IR drops Area bonding - On chip bypass capacitors, Power supply isolation - Noise sources in digital system, Power supply Noise - Cross talk, Inter - symbol interference.

Unit III: Signaling convention and Circuits **9 Hours**

Signaling modes for transmission lines - Signaling over lumped transmission media, Signaling over RC interconnects, driving lossy LC lines- Terminators, transmitter and receiver circuits.

Unit IV: Timing Convention and Synchronization **9 Hours**

Timing fundamentals - Timing properties of clocked storage elements -Signals and events, Open loop Timing - Level sensitive clocking - Pipeline timing - Closed loop Timing - Clock Distribution, Synchronization failure - Electromagnetic Compatibility.

Unit V: Instructional Activities **9 Hours**

Study the characteristics of Transmission lines - Noise sources - ISI by simulation and measure ISI by CRO.

Reference Books:

1. William S. Dally and John W. Paulton, Digital System Engineering, Cambridge University Press, 2008.
2. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley Publishing Company, 1996.
3. Jan M. Rabaey et al., Digital Integrated Circuits: A Design Perspective, 2nd Edition PHI, 2003.
4. Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI Design, Prentice Hall, 1994.
5. Alfred L Crouch, Design for Test for Digital ICs and Embedded Core Systems, Prentice Hall, 1999.
6. Howard Johnson and Martin Graham, High Speed Digital Design A Hand book of Black Magic, Prentice Hall PTR,1993
7. Gelyer, Allen and Strider, VLSI Design Techniques for Analog and Digital Circuits, McGraw Hill, 2008.

Hyperlinks:

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixed signal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

VEENG 552

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 553	PRINCIPLES OF ASIC DESIGN	2	1	0	3	45

Prerequisite : Digital VLSI Design

Objective : To make the students to understand the architectural details of programmable ASICs including logic synthesis, floor-planning, placement and routing.

Outcome : The students will be able to gain sufficient theoretical knowledge for carrying out ASIC and FPGA design.

Unit I: Introduction to Programmable Devices **9 Hours**

Programmable logic devices: ROM - PLA - PAL - PLD - FPGA - features, programming and applications using complex programmable logic devices; Speed performance and system programmability.

Unit II: Introduction to ASIC **9 Hours**

Design flow - types of ASICs - full custom with ASIC - semi custom ASICs - standard cell based ASIC - gate array based ASIC - channeled - channel less - structured - data path elements - adders - multiplier - cell compilers ; Logical effort : area and efficiency - paths - multi stage cells - optimum delay.

Unit III: Low Level Design Language **9 Hours**

EDIF: PLA tools - introduction to CFI designs representation; Half gate ASIC: Introduction to synthesis and simulation - two level logic synthesis - high level logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

Unit IV: Floor Planning, Placement and Routing **9 Hours**

Physical design: CAD tools - system partitioning - estimating ASIC size - partitioning methods; Floor planning tools - I/O and power planning - clock planning - placement algorithms - iterative placement improvement; Time driven placement methods - physical design flow global routing - local routing - detail routing - special routing - circuit extraction and DRC.

Unit V: Instructional Activities **9 Hours**

Spartan 3E and Vertex Board Analysis - inputs and outputs - clock and power inputs - Xilinx I/O blocks - PLAs and PALs design using ASIC board.

Reference Books:

1. Smith M J S, Application Specific Integrated Circuits, Pearson Education, 2009.
2. Farzad N and Faranak N, From ASICs to SOCs: A Practical Approach, Prentice Hall, 2003.
3. Rajsuman R, System-on–a–Chip: Design and Test, Artech House, 2000.
4. Farzad N, Timing Verification of Application Specific Integrated Circuits, 1st Edition, Prentice Hall, 1999.

Hyperlink:

1. en.wikipedia.org/wiki/Standard_cell
2. www.utdallas.edu/~zhoud/DesignEntry
3. en.wikipedia.org/wiki/High-level_synthesis

VEENG 553

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 554	REAL TIME SYSTEMS	2	1	0	3	45

Prerequisite : Basic Knowledge in Operating System and Microcontrollers

Objective : To provide the fundamental concepts in real time systems and basic multi-task scheduling algorithms

Outcome : Understand the concept of multi-task scheduling algorithms for various tasks as well as understand the impact of the latter two on scheduling

Unit I: Introduction **9 Hours**

Introduction : Issues in Real Time Computing – Structure of a Real Time System – Task classes Performance Measures for Real Time Systems – Estimating Program Run Times – Characteristics of Real-time Systems – Classification of Real-time systems – Applications of Real-time Systems – Safety and Reliability. Basic Concepts of Scheduling: Real-time applications - Basic concepts for real-time task scheduling. Scheduling of Independent Tasks: Basic on-line algorithms for periodic tasks - Hybrid task sets scheduling.

Unit II: Scheduling in Real-Time Systems **9 Hours**

Scheduling of Dependent Tasks: Tasks with precedence relationships - Tasks sharing critical resources. Scheduling schemes for handling overload: Scheduling techniques in overload conditions - Handling real-time tasks with varying timing parameters - Handling overload conditions for hybrid task sets. Multiprocessor scheduling and comparison with uniprocessor scheduling

Unit III: Programming Language And Tools **9 Hours**

Programming Languages and Tools – Desired language characteristics – Data typing – Control structures Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling – Overloading and Generics – Multitasking – Low level programming – Task Scheduling – Timing Specifications

Unit IV: Real Time Databases **9 Hours**

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

Unit V: Instructional Activities **9 Hours**

Study of operating System-Threads and Tasks-The Kernel, Time Services and Scheduling

Mechanisms, other basic operating functions-Communication and Synchronization Application program interface and SSP structure.

Reference Books:

1. C. M. Krishna and Kang G. Shin, Real-Time Systems, McGraw Hill International Editions, 1997.
2. Stuart Bennett, Real Time Computer Control, 2nd Edition, Pearson Education Ltd., 2012.
3. Francis Cottet, Joelle Delacroix and Zoubir Mammeri, Scheduling in Real Time Systems, John Wiley & Sons Ltd., 2002.
4. Rajib Mall, Real-Time Systems: Theory and Practice, Pearson Education, 2008.
5. TimeSys Corporation, The Concise Handbook of Real Time Systems, TimeSys Corporation, Pittsburgh, PA, 2002.
6. Peter D. Lawrence, Real Time Micro Computer System Design – An Introduction, McGraw Hill, 1988.
7. Spyros G Tzafestas and J K Pal, Real Time Microcomputer Control of Industrial Processes, Kluwer Academic Publishers, The Netherlands, 1990.
8. Jane W. S. Liu, Real Time System, Pearson Edition, 2002.

Hyperlinks:

1. nptel.ac.in/courses/106105036
2. http://www.slideshare.net/sanjivmalik/rtos-concepts

VEENG 554

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 555	RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	2	1	0	3	45

Prerequisite : Basic knowledge in Microprocessor and its Architecture

Objective : To introduce techniques for altering the existing processor architecture to suit recent developments.

Outcome : To analyze and develop RISC based architecture with protection techniques.

Unit I: AVR Microcontroller Architecture **9 Hours**

Architecture: memory organization – Addressing modes – Instruction set – Programming Techniques –Assembly language & C programming- Development Tools – Cross Compilers – Hardware Design Issues.

Unit II: Peripheral Of AVR Microcontroller **9 Hours**

I/O Memory – EEPROM – I/O Ports –SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing.

Unit III: ARM Architecture and Programming **9 Hours**

Arcon RISC Machine – Architectural Inheritance – Core & Architectures - Registers – Pipeline - Interrupts – ARM organization - ARM processor family – Co-processors. Instruction set – Thumb instruction set – Instruction cycle timings - ARM Programmer's model – ARM Development tools – ARM Assembly Language Programming and 'C' Compiler Programming.

Unit IV: ARM Application Development **9 Hours**

Introduction to DSP on ARM : FIR Filter – IIR Filter – Discrete fourier transform – Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Example: Standalone - Embedded Operating Systems – Fundamental Components - Example Simple little Operating System

Unit V: Instructional Activities **9 Hours**

Interfacing of various I/O devices and memory with ARM processor for home automation

Reference Books:

1. Steve Furber, ARM System on Chip Architecture, 2nd Edition, Addision Wesley Longman, 2011.
2. Andrew N. Sloss, Dominic Symes, Chris Wright and John Rayfield, ARM System. Developer's Guide Designing and Optimizing System Software, Elsevier Science, 2016.
3. Trevor Martin, The Insider's Guide To The Philips ARM7-Based Microcontrollers, An Engineer's Introduction To The LPC2100 Series, Hitex (UK) Ltd., 2005.
4. Dananjay V. Gadre, Programming and Customizing the AVR Microcontroller, McGraw Hill, 2001.
5. Lyla B Das, The X86 Microprocessors: Architecture and Programming, Pearson Education India, 2010.
6. Sivarama P. Dandamudi, Guide to RISC Processors, Springer, 2005.

Hyperlinks:

1. http:// www.nptel.iitm.ac.in
2. http://www.avr.com
3. http://www.arm.com

VEENG 555

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 556	TESTING OF VLSI CIRCUITS	2	1	0	3	45

Prerequisite : Basic knowledge in VLSI circuit design

Objective : To understand logic fault models and test generation for sequential and combinational logic circuits

Outcome : Gain more knowledge in the identification of faults in logic circuits with various fault models and various testing algorithms.

Unit I: Testing and Fault Modelling **9 Hours**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

Unit II: Test Generation **9 Hours**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

Unit III: Design for Testability **9 Hours**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design.

Unit IV: Self Test and Test algorithms **9 Hours**

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test generation for Embedded RAMs.

Unit V:Instructional Activities **9 Hours**

Fault modelling – Test algorithm – Automatic test generation– Scan based design – Self test – Fault identification.

Reference Books:

1. A. L. Crouch, Design Test for Digital ICs and Embedded Core Systems, Prentice Hall International, 2002.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems and Testable Design, Jaico Publishing House, 2002.
3. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits, Kluwer Academic Publishers, 2006.
4. P. K. Lala, Digital Circuit Testing and Testability, Academic Press, 2002.

Hyperlink:

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in

VEENG 556

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 557	VLSI SIGNAL PROCESSING	2	1	0	3	45

Prerequisite : Knowledge in Digital Signal Processing

Objective : To introduce techniques for signal processing based architecture to suit VLSI implementation.

Outcome : Gain knowledge in various architecture for VLSI signal processing

Unit I: Parallel processing in FIR filter Realization **9 Hours**

DSP systems: Programs- Applications- Representation- Data flow graphs; Loop Bound and Iteration Bound- Algorithms- Iteration Bound of Multirate Data-flow graphs- Pipelining of FIR filters- Parallel Processing of FIR filters.

Unit II: Systolic Architecture Design **9 Hours**

Retiming : properties- applications- Solving inequality systems- Retiming techniques- Unfolding- algorithm- application- properties- Critical path- Folding transformation, Techniques- Folded architectures- Folding of Multirate systems- Systolic architecture design methodology- FIR systolic arrays- Scheduling vector- Matrix-Matrix multiplication- Systolic design for space representations with delays.

Unit III: Efficient Realization of IIR filters in DSP **9 Hours**

Fast convolution algorithms: Iterated- Cyclic Convolutions- Design by Inspection- DCT and Inverse DCT- Parallel architectures for rank -order filters- Pipeline interleaving in digital filters- Pipelining in 1^{st}-order and higher-order IIR Digital Filters- Parallel processing for IIR Filters- Combined pipelining and parallel processing for IIR Filters.

Unit IV: Finite Word Length Effect in Pipelined Architecture **9 Hours**

Scaling and Round off noise: State variable description- Scaling and Round-off noise computation- Round off noise in pipelined IIR filters- Round off noise computation using state variable- Slow-Down- Retiming and Pipelining- Fast binary adders and multipliers- Parallel multipliers.

Unit V: Instructional Activities **9 Hours**

Design and simulate FIR and IIR filters for the given specifications study of finite word length effect in different realization

References Books:

1. K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, Wiley, 2009.
2. M. Ismail and T. Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 2004.

Hyperlinks:

1. http:// www.nptel.iitm.ac.in
2. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals

VEENG 557

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 630	ADVANCED EMBEDDED SYSTEM	2	1	0	3	45

Prerequisite : Knowledge in embedded system

Objective : To provide the fundamentals on design attributes of functional units of a Processor and Hardware software partitioning in system design

Outcome : Understand the timing and interrupt in processor, the memories and communication protocol in embedded field and design a simple processor model

Unit I: Introduction to Embedded Hardware and Software **9 Hours**

Terminology - Gates - Timing diagram - Memory - Microprocessor buses - Direct memory access - Interrupts - Built interrupts - Interrupts basis : Shared data problems - Interrupt latency - Embedded system evolution trends - Interrupt routines in an RTOS environment.

Unit II: System Modeling With Hardware/Software Partitioning **9 Hours**

Embedded systems: Hardware/Software Co-Design, Co-Design for System Specification and modeling- Single-processor Architectures and Multi-Processor Architectures, comparison of Co Design Approaches; Models of Computation, Requirements for Embedded System Specification - Hardware/Software Partitioning Problem- Hardware/Software Cost Estimation- Generation of Partitioning by Graphical modeling- Formulation of the HW/SW scheduling, Optimization.

Unit III: Hardware/Software Co-Synthesis **9 Hours**

The Co-Synthesis Problem- State-Transition Graph- Refinement and Controller Generation- Distributed System Co-Synthesis.

Unit IV: Memory And Interfacing **9 Hours**

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

Unit V: Instructional Activities **9 Hours**

Design Process Model- Embedded System modeling with Hardware/Software Partitioning. Develop a model arbitration multilevel bus architecture and digital camera

Reference Books:

1. David. E. Simon, An Embedded Software Primer, Pearson Education, 2012.
2. Tammy Noergaard, Embedded System Architecture, A comprehensive Guide for Engineers and Programmers, Elsevier, 2008.
3. Raj Kamal, Embedded Systems - Architecture, Programming and Design, Tata McGraw Hill, 2012.
4. Frank Vahid and Tony Gwargie, Embedded System Design, John Wiley and Sons, 2014.
5. Steve Heath, Embedded System Design, Elsevier, 2nd Edition, 2004.
6. Ralf Niemann, Hardware/Software Co-Design for Data Flow Dominated Embedded Systems, Kluwer Academic Publications, 1998.
7. Jorgen Staunstrup and Wayne Wolf, Harware/Software Co-Design: Principles and Practice, Kluwer Academic Publications, 1997.
8. Giovanni De Micheli and Rolf Ernst Morgon, Reading in Hardware/Software Co-Design, Kaufmann Publishers, 2001.

Hyperlinks:

1. www.vectorindia.org/embedded_coursecontent.html
2. www.cetpainfotech.com
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com

VEENG 560

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 631	ADVANCED IMAGE PROCESSING	2	1	0	3	45

Prerequisite : Fundamentals of Signals and Systems

Objective : Make the students to understand the concepts used in image processing techniques and its analysis.

Outcome : Students will be able to work with various image processing techniques for real time applications.

Unit I: Digital Image Fundamentals **9 Hours**

Image fundamentals: Image acquisition - sampling and quantization - image resolution- basic relationship between pixels - color images - RGB, HSI and other models; Transform based models (DFT, DCT, DWT); Image Enhancement: Spatial and frequency averaging - smoothening and sharpening filters.

Unit II: Segmentation and Denoising **9 Hours**

Image Segmentation: Edge detection - edge linking via Hough transform - thresholding- region based segmentation; Denoising: Maximum likelihood estimation - Bayesian estimators - model selection (MDL principle) - transform based denoising - adaptive wiener filtering - soft shrinkage and hard thresholding.

Unit III: Image Compression **9 Hours**

Image compression: Basics of source coding theory (lossless and lossy) - Vector quantization - codebook design - transform and sub band coding.

Unit IV: Image security and forensic **9 Hours**

Image Security: cryptography and steganography techniques- Chaos based and Non-Chaos based methods; Image Forensics: Key photographic techniques-detection techniques for crime scene analysis.

Unit V: Instructional Activities **9 Hours**

Simulation of preprocessing techniques-implementation of image processing techniques for real time applications-forensic analysis using related tools.

Reference Books:

1. Rafael C Gonzalez and Richard E Woods, Digital Image Processing, 2nd Edition, Pearson Education, 2004.
2. Anil K Jain, Fundamentals of Digital Image Processing, 3rd Edition, Pearson Education, 2002.
3. William K Pratt, Digital Image Processing, 2nd Edition, John Wiley, 2002.
4. Milan Sonka et al., Image Processing, Analysis and Machine Vision, 2nd Edition, Vikas Publishing House, 1999.
5. Prabat K Andleigh and Kiran Thakrar, Multimedia Systems and Design, Prentice Hall India, 2007.
6. Tay Vaughan, Multimedia Making It Work, McGraw Hill, 2011.
7. Parekh R, Principles of Multimedia, Tata McGraw Hill, 2006.
8. Robinson and Edward, Introduction to Crime Scene Photography, Elsevier/Academia Press, 2012.
9. Herbert Blitzer, Karen Stein-Ferguson and Jeffrey Huang, Understanding Forensic Digital Imaging, 1st Edition, Academic Press, 2008.

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1. www.imageprocessingplace.com/DIP-3E/dip3e_main_page.html
2. https://www.tutorialspoint.com/dip/
3. https://homepages.inf.ed.ac.uk/rbf/HIPR2/glossary.htm

VEENG 631

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 632	CAD FOR VLSI CIRCUITS	2	1	0	3	45

Prerequisite : Basic knowledge in data structure algorithms

Objective : To Understand VLSI design automation tools

Outcome : Can understand Simulation and Logic Synthesis in VLSI design automation.

Unit I: Introduction to VLSI Design Flow **9 Hours**

Introduction to VLSI Design methodologies: Basics of VLSI design automation tools- Algorithmic Graph Theory and Computational Complexity- Tractable and Intractable problems- General purpose methods for combinatorial optimization.

Unit II: Layout, Placement And Partitioning **9 Hours**

Layout Compaction- Design rules- Problem formulation- Algorithms for constraint graph compaction- Placement and partitioning- Circuit representation- Placement algorithms- Partitioning.

Unit III: Floor Planning And Routing **9 Hours**

Floor planning concepts: Shape functions and floor plan sizing- Types of local routing problems- Area routing- Channel routing- Global routing- Algorithms for global routing.

Unit IV: Simulation and Logic Synthesis **9 Hours**

Simulation- Gate-level modeling and simulation-Switch-level modeling and simulation- Combinational Logic Synthesis- Binary Decision Diagrams- Two Level Logic Synthesis.

Unit V: Instructional Activities **9 Hours**

Study of Hardware models for high level synthesis, internal representation- allocation- assignment and scheduling- scheduling algorithms- Assignment problem- High level transformations.

Reference Books:

1. N. A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic Publishers, 2002.
2. S. H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2002.
3. Sadiq M. Sait and Habib Youssef, VLSI Physical Design Automation: Theory and Practice, World Scientific 1999.
4. Steven M.Rubin, Computer Aids for VLSI Design, Addison Wesley Publishers, 1987.
5. Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2010.
6. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Springer International Edition, 2005.

Hyperlinks:

1. www.facweb.iitkgp.ernet.in/~isg/CAD/index.html
2. nptel.ac.in/courses/106106088/

VEENG 632

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 633	DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS	2	1	0	3	45

Prerequisite : Basics of semiconductor device operation and VLSI design.

Objective : To study analog integrated circuits features design and analysis methods of analog and mixed mode VLSI circuits.

Outcome : Students will be able to design efficient analog and mixed mode VLSI circuits.

Unit I: Data Converters **9 Hours**

Data Converter Fundamentals: Analog versus digital discrete time signals - converting analog signals to data signals- sample and hold characteristics - DAC specifications - ADC specifications - mixed-signal layout issues.

Unit II: Data Converter Architectures **9 Hours**

Data Converter Architectures: DAC architectures - digital input code - resistors string - R-2R ladder networks - current steering - charge scaling 0 DACs - cyclic DAC - pipeline DAC - ADC architectures – flash ADC - 2-step flash ADC - pipeline ADC - integrating ADC - successive approximation ADC.

Unit III: SNR in Data Converters **9 Hours**

Data Converter SNR: Improving SNR using averaging (Excluding Jitter & averaging onwards) - decimating filters for ADCs (Excluding Decimating without Averaging onwards) - interpolating filters for DAC - band pass and high pass sync. filters.

Unit IV: Operational Amplifiers and Mixed Signal Circuits **9 Hours**

Differential amplifier: basic differential pair - Gilbert Cell; Op-Amp: Performance parameters - one stage and two stage Op-Amp - design of two stage Op-Amps - gain boosting - common mode Feedback - slew rate - offset effects - PSRR- noise - stability and frequency compensation - two stage open loop comparators–high speed comparators - sample and hold circuit- switched capacitor circuits - oscillators - VCO - PLL.

Unit V: Instructional Activities **9 Hours**

Design and simulation of different VLSI Circuits: Current mirrors - Differential Amplifier - PLL - ADC/DAC

Reference Books:

1. Razavi B, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill Edition, 2008.
2. Baker R J, CMOS: Circuit Design, Layout and Simulation, 3rd Edition, John Wiley and Sons, NJ, 2010.
3. Allen P E and Holberg D R, CMOS Analog Circuit Design, 3rd Edition, Oxford University Press, USA, 2012.
4. Baker R J, CMOS: Mixed-Signal Circuit Design, John Wiley India Edition, 2009.

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1. http://nptel.ac.in/courses/117101105/
2. http://nptel.ac.in/courses/117101106/
3. http://nptel.ac.in/courses/117106034/
4. http://nptel.ac.in/courses/117106030/

VEENG 633

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 634	DISTRIBUTED EMBEDDED COMPUTING	2	1	0	3	45

Prerequisite : Knowledge in Data Communication Networks and Microcontrollers

Objective : To provide knowledge in distributed embedded computing architecture

Outcome : Gain knowledge in distributed embedded computing architecture.

Unit I: Internet Infrastructure **9 Hours**

Broad Band Transmission facilities - Open Interconnection standards -Local Area Networks - Wide Area Networks -Network management - Network Security - Cluster computers.

Unit II: Internet Concepts **9 Hours**

Capabilities and limitations of the internet - Interfacing Internet server applications to corporate databases HTML and XML Web page design through programming and the use of active components.

Unit III: Embedded Java **9 Hours**

Introduction to Embedded Java and J2ME - embedded java concepts - IO streaming - Object serialization - Networking - Threading - RMI - multicasting - distributed databases - Smart Card basics - Java card technology overview Java card objects - Java card applets - Web Technology for Embedded Systems.

Unit IV: Embedded Agent **9 Hours**

Introduction to the embedded agents - Embedded agent design criteria - Behaviour based, Functionality based embedded agents - Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

Unit V: Instructional Activities **9 Hours**

The product concepts- Automotive -Engine Control- Modeling the design of the Product Concept- Embedded System design and development life cycle model- Creating a basic VHDL for the entity of the memory block- Arithmetic and logic Unit.

References Books:

1. Dietel and Dietel, JAVA How to Program, Prentice Hall 1999.
2. Sape Mullender, Distributed Systems, Addison Wesley, 1993.
3. George Coulouris and Jean Dollimore, Distributed Systems: Concepts and Design, Addison Wesley 1988.
4. Bernd Kleinjohann, Architecture and Design of Distributed Embedded Systems, Kluwer Academic Publisher, Boston, April 2001.
5. Wigglesworth, Java Programming Advanced Topics, Cengage, 2010.
6. Mclaughlin, Java and XML,O'Reilly, 2006.
7. Jack Ganssle, Embedded Systems, Elsevier Publication, 2008.
8. Tammy Noergaard, Embedded Systems Architecture, Elsevier Publications, 2005.

Hyperlinks:

1. http://www.oracle.com/technetwork/articles/javase/rmi-corba-136641.html
2. http://www.es.ele.tue.nl/~heco/courses/ECA/index.html
3. www.pa.icar.cnr.it/cossentino/AOSETF10/docs/jamont.ppt
4. http://philip.greenspun.com/panda/databases-interfacing
5. C/C++ users Journal-http://www.cuj.com/
6. C++ Report-http://www.creport.com/
7. Design News-http://www.designnews.com/

VEENG 634

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 635	HARDWARE SOFTWARE CO-DESIGN	2	1	0	3	45

Prerequisite : Basic knowledge of testing techniques in Embedded System

Objective : To learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.

Outcome : Gain knowledge in the fundamental building blocks of the hardware and software co-design and related implementation, testing environments, techniques and their inter-relationships

Unit I: System Specification and Modeling **9 Hours**

Embedded Systems : Hardware/Software Co-Design - Co-Design for System Specification and Modelling- Co-Design for Heterogeneous Implementation - Processor Synthesis - Single-Processor Architectures with one ASIC - Single-Processor Architectures with many ASICs- Multi-Processor Architectures, Comparison of Co-Design Approaches - Models of Computation -Requirements for Embedded System Specification

Unit II: Hardware/Software Partitioning **9 Hours**

The Hardware/Software Partitioning Problem- Hardware-Software Cost Estimation- Generation of the Partitioning Graph- Formulation of the HW/SW Partitioning Problem, Optimization- HW/SW Partitioning based on Heuristic Scheduling- HW/SW Partitioning based on Genetic Algorithms.

Unit III: Hardware/Software Co-Synthesis **9 Hours**

The Co-Synthesis Problem- State-Transition Graph- Refinement and Controller Generation- Distributed System Co-Synthesis.

Unit IV: Prototyping and Emulation **9 Hours**

Introduction: Prototyping and Emulation Techniques - Prototyping and Emulation Environments- Future Developments in Emulation and Prototyping -Target Architecture- Architecture Specialization Techniques -System Communication Infrastructure- Target Architectures and Application System Classes- Architectures for Control-Dominated Systems- Architectures for Data-Dominated Systems-Mixed Systems and Less Specialized Systems

Unit V: Instructional Activities **9 Hours**

Design a System Level Synthesis- by learning the basics of the Xilinx Vivado High Level Synthesis (HLS) CAD Flow: Design Entry- Compiling and Simulation- Create a complete Hardware/Software Co-design that integrates the Arm Processor with an IP.

Reference Books:

1. Ralf Niemann, Hardware/Software Co-Design for Data Flow Dominated Embedded Systems, Kluwer Academic Publisher, 1998.
2. Jorgen Staunstrup and Wayne Wolf, Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Publisher, 1997.
3. Giovanni De Micheli and Rolf Ernst Morgon, Reading in Hardware/Software Co-Design, Kaufmann Publishers, 2001.

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1. https://www.slideshare.net/destruck/hardware-software-codesign-16146924
2. https://www.cs.ccu.edu.tw/~pahsiung/.../notes/SoC_Design_Flow_Tools_Codesign.pdf

VEENG 635

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 636	MICRO-ELECTRO MECHANICAL SYSTEMS	2	1	0	3	45

Prerequisite : Knowledge in design of electronic and microwave circuits

Objective : To familiarize the student with the technology and applications of Micro-Electro Mechanical Systems (MEMS).

Outcome : Students will be able to design different types of MEMS based devices, circuits and subsystems.

Unit I: Introduction to MEMS **9 Hours**

Evolution of Micro Electro Mechanical Systems (MEMS): Driving force for MEMS development - MEMS material properties - microelectronics technology for MEMS; The Finite Element Method: Important mathematical and physical concept in FEM - discretization and other approximation.

Unit II: Micromachining Technology for MEMS **9 Hours**

Fabrication Process: MEMS fabrication technologies - bulk micro machining - surface micro machining - LIGA process; Bonding and packing of MEMS - MEMS reliability - scaling in MEMS; Recent research direction in MEMS: CMOS- MEMS integration - polymer MEMS - NEMS etc.

Unit III: Sensor and Actuators **9 Hours**

Sensors: Classifications - principle - design and characterization of thermal – micromachined - mechanical - pressure - flow sensor - bio– sensor; Actuation in MEMS Devices: Electrostatic actuation - parallel plate capacitor - cantilever beam based movement; MEMS accelerometers; optical MEMS: Micro mirror.

Unit IV: RF MEMS **9 Hours**

Switches: Cantilever MEMS based switch; Inductors and Capacitors: Modeling and design issues of planar inductor and capacitors; RF Filters: Modeling of mechanical filters; Phase Shifters: Classifications and limitations; Micro Machined Antennas: Micro-strip antennas - design parameters.

Unit V: Instructional Activities **9 Hours**

Modeling, simulation and analysis in the applications of MEMS switch, sensors and actuators using related platform.

Reference Books:

1. Madou M, Fundamentals of Micro Fabrication, CRC Press, 3rd Edition, 2011.
2. Senturia, Micro System Design, Kluwer, 2007.
3. Maluf N and Williams K, An Introduction to Micro-electromechanical Systems Engineering, Artech House, 2nd Edition, 2004.
4. Varadan V K, Vinoy K J and Jose K A, RF MEMS and Their Applications, Wiley and Sons, 2003.
5. Rebeiz G, RF MEMS: Theory, Design, and Technology, Wiley/ IEEE Press, 2004.
6. Robert D C, Finite Element Modeling for Stress Analysis, John Wiley and Sons, 1995.

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1. http://freevideolectures.com/blog/2010/11/130-nptel-iit-online-courses/#
2. http://biomedikal.in/2011/02/lecture-notes-on-mems-technology/
3. http://www.learnerstv.com/Free-engineering-Video-lectures-ltv122-Page1.html

VEENG 636

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 637	NANOELECTRONICS	2	1	0	3	45

Prerequisite : Basic knowledge of electronic devices and its structures.

Objective : To introduce the characteristics and applications of nanoelectronic devices and its characteristics

Outcome : Familiar with certain nanoelectronic systems and building blocks such as: low-dimensional semiconductors, heterostructures, carbon nanotubes, quantum dots, nanowires etc.

Unit I: Introduction **9 Hours**

Particles - waves - Wave mechanics - Schrodinger equation, free and confined electrons- particle statistics and density of states. Electron transport in semiconductors and nanostructures - Quantum dots- Quantum Well - Quantum wire - materials and its properties - Ballistic electron transport- 1D transport -Spin electronics- Electrical and Electronics Applications of Nanotechnology

Unit II: Nanoscale CMOS **9 Hours**

Survey of modern electronics and trends towards nanoelectronics CMOS scaling, challenges and limits, static power, device variability, interconnect - CNT-FET, HEMT, pHEMT FinFET, Ferro FET nanoscale CMOS circuit design and analysis

Unit III: NanoElectronic Structure And Devices **9 Hours**

Resonant-tunneling diodes - Resonant Tunneling Transistor- Single-electron transfer devices- Potential effect transistors - Quantum-dot cellular automata, NanoPhotonic Devices-Molecular electronic devices - Nanoelectromechanical system devices

Unit IV: NanoElectronic Memories **9 Hours**

Nanotube for memories - Nano-RAM - Nanoscale DRAM, SRAM, Tunnel magneto resistance- Giant magneto resistance- design and applications.

Unit V: Instructional Activities **9 Hours**

Assignment and presentation on Nanolithography-Importance of micro/nanopatterning-Classification of lithographic techniques-Photolithography - A conventional and classical method - Ion beam Lithography -X-ray lithography -Electron beam lithography-Alternate Nanolithographic Techniques

Reference Books:

1. George W. Hanson, Fundamental of NanoElectronics, Pearson Education, 2008.
2. Michael A. Nielsen and Isaac L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2000.
3. Adrian Ionesu and Kaustav Banerjee eds. Emerging Nanoelectronics: Life with and after CMOS, Vol. I, II and III, Kluwer Academic Publishers, 2005.
4. Kiyoo Itoh Masashi Horiguchi and Hitoshi Tanaka, Ultra Low Voltage NanoScale Memories, 7th Edition, Kindle Edition, Springer, 2007.

Hyperlinks:

1. onlinelibrary.wiley.com › Materials Science › Analysis/Characterization of nanosystems
2. https://www.fisgeo.unipg.it/~luca.../fisinfo/.../Electronics-beyond-nanoscale-cmos.pdf

VEENG 637

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 638	PERVASIVE DEVICES AND TECHNOLOGY	2	1	0	3	45

Prerequisite : Knowledge in Wireless networks and Mobile communication devices

Objective : To expose the fundamentals of pervasive computing and security in mobile computing

Outcome : Can design and deploy wireless sensor networks for specific applications

Unit I: Introduction **9 Hours**

Ubiquitous or Pervasive Computing - Context - Definitions and types Context–aware Computing and Applications - Mobile computing-Networks- Middleware and gateways- Applications and services- Developing mobile computing applications- Architecture for mobile computing- Design considerations for mobile computing.

Unit II: Pervasive Networking **9 Hours**

Introduction, Networking Infrastructure and Architecture of PERV NET, Mobility management, service discovery, disconnected operation, Dynamic configuration, auto registration, content based routing, Backbone Technology: Electrical Backbone Networks - Optical Backbone Networks – Wireless Backbone Networks – Wireless Access Technology - Pervasive Web Application architecture- Access from PCs and PDAs - Access via WAP

Unit III: Pervasive Devices **9 Hours**

Introduction with Case study of - PDA - Mobile Phone: Elements - Mobile Information Architecture - Mobile Phone Design - Android Overview - The Stack - Android User Interface - Preferences, the File System, the Options Menu and Intents.

Unit IV: Wireless Devices and Security Issues In Mobile Computing **9 Hours**

Mobile phones-PDA-Design constraints in applications for handheld devices - Convergence technologies-Call routing-Voice over IP applications-IMS-Mobile VoIP. Security in mobile computing- Issues- Security Protocols-models-Security framework for mobile environment.

Unit V:Instructional Activities **9 Hours**

Case study on Emerging Wireless Technologies , IEEE 802.20 Mobile Broadband Wireless Access

References Books:

1. Asoke K Talukder and Roopa R Yavagal, Mobile Computing, Tata McGraw Hill, 2010.
2. Frank Adelstein, Sandeep K S Gupta, Golden G Richard III and Loren Schwiebert, Fundamentals of Mobile and Pervasive Computing, Tata McGraw Hill, 2007.
3. Jochen Burkhardt, Horst Henn, Stefan Hepper, Klaus Rindtorff and Thomas Schack, Pervasive Computing: Technology and Architecture of Mobile Internet Applications, Addison Wesley, 2002.
4. Uwe Hansmann, L. Merk, M. Nicklous, T. Stober and U. Hansmann, Pervasive Computing (Springer Professional Computing), Springer Verlag, 2003.
5. Debashis Saha and Amitava Mukherjee, Networking Infrastructure for Pervasive Computing, Springer International Edition, 2011.

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1. https://en.wikipedia.org/wiki/Ubiquitous_computing
2. http://www.nptel.iitm.ac.in/courses
3. https://www.isoc.org

VEENG 638

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 639	ROBOTICS AND AUTOMATION	2	1	0	3	45

Prerequisite : Basic knowledge in electrical machines, electronic devices and microcontroller

Objective : To educate on formulation of manipulator Jacobians and introduce path planning Techniques and to introduce robot control techniques and Robotic applications

Outcome : It will provide a comprehensive educational environment and enable students to gain expertise in next generation robotics and automation systems

Unit I: Introduction **9 Hours**

Definition-Classification-History - Robots components-Degrees of freedom-Robot joints-coordinates - Reference frames-workspace - actuators-sensors - Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors-proximity and range sensors- vision system-social issues

Unit II: Robot Arm Kinematics **9 Hours**

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

Unit III: Robot Arm Dynamics **9 Hours**

Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion

Unit IV: Robot Applications **9 Hours**

Material Transfer & Machine Loading / Unloading - General Consideration in robot material handling transfer applications – Machine loading and unloading.

Processing Operations: Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

Unit V: Instructional Activities **9 Hours**

Design and develop robotic arm using ARM processor - Line follower models

Reference books:

1. R. K. Mittal and I. J Nagrath, Robotics and Control, Tata McGraw Hill, 4th Reprint 2003.
2. Saeed B. Niku, Introduction to Robotics, Pearson Education, 2002.
3. Fu, K. S. Gonazlez R C and Lee C S G, Robotics: (Control, Sensing, Vision and Intelligence), McGraw Hill, 1987.
4. Wesley E and Snyder R, Industrial Robots, Computer Interfacing and Control, Prentice Hall International Edition, 1988.
5. Philippe Coiffet, Robot Technology Vol. II (Modelling and Control), Prentice Hall Inc., 1983.
6. Groover M P and Mitchell Weiss, Industrial Robotics Technology Programming and Applications, Tata McGraw Hill, 1986.
7. John J. Craig, Introduction to Robotics: Mechanics and Control, Prentice Hall Inc., 1989.

Hyper Links:

1. http:// www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu
3. http://web.iiit.ac.in/~bezawada/CN.html

VEENG 639

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 640	SYSTEM- ON-CHIP DESIGN	2	1	0	3	45

Prerequisite : Basic knowledge in Processor Architecture

Objective : To learn System on chip fundamentals, their applications and to learn the various computation models of SOCs

Outcome : Students will be able to discuss System-on-chip fundamentals, their applications and On-chip networking methods.

Unit I: Introduction **9 Hours**

System Architecture: Components of the system- Hardware & Software- Processor Architectures- Memory and Addressing- System level interconnection- An approach for SOC Design, System Architecture and Complexity.

Unit II: Processors **9 Hours**

Introduction: Processor Selection for SOC- Basic concepts in Processor Architecture- Basic concepts in Processor Micro Architecture- Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays- Branches- More Robust Processors- Vector Processors and Vector Instructions extensions= VLIW Processors, Superscalar Processors.

Unit III: Memory Design For SOC **9 Hours**

Overview of SOC external memory: Internal Memory- Size- Scratchpads and Cache memory- Cache Organization- Cache data- Write Policies- Strategies for line replacement at miss time- Types of Cache- Split – I, and D – Caches- Multilevel Caches- Virtual to real translation - SOC Memory System- Models of Simple Processor - memory interaction**.**

Unit IV: Interconnect Customization And Configuration **9 Hours**

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses - Analytic Bus Models- SOC Customization: An overview- Customizing Instruction Processor- Reconfiguration Technologies- Mapping design onto Reconfigurable devices-Instance- Specific design- Customizable Soft Processor- Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Unit V:Instructional Activities **9 Hours**

SOC Design approach: simulate and verify AES algorithms- design and evaluation of Image compression - JPEG compression.

References Books:

1. Michael J Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiely India Pvt., Ltd., 2012.
2. Steve Furber, ARM System on Chip Architecture, 2nd Edition, Addison Wesley Professional 2001.
3. Ricardo Reis, Design of System on a Chip: Devices and Components, Kluwer Academic Publishers, 2004.
4. Jason Andrews and Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Bk and CD-ROM.
5. Prakash Rashinkar, Peter Paterson and Leena Singh L, System on Chip Verification Methodologies and Techniques, Kluwer Academic Publishers, 2007.

Hyperlinks:

1. http://ic.sjtu.edu
2. http://nptel.iitm.ac.in

VEENG 640

Course Code	Name of the Course	Periods			Credits	Total Hours
		L	T	P		
VEENG 641	VLSI FOR WIRELESS COMMUNICATION	2	1	0	3	45

Prerequisite : Knowledge in Analog and Digital Communication

Objective : To study the design concepts of low noise amplifiers and to study the various types of mixers designed for wireless communication.

Outcome : Understanding of application of VLSI circuits in wireless communication.

Unit I: Components and Devices **9 Hours**

Integrated inductors- resistors- MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

Unit II: Mixers **9 Hours**

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer

Unit III: Frequency Synthesizers **9 Hours**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

Unit IV: Sub Systems **9 Hours**

Data converters in communications, adaptive Filters, equalizers and transceivers.

Unit V: Instructional Activities **9 Hours**

Simulation for different Mixer circuits and Frequency Synthesizers using the appropriate simulation tool.

Reference Books:

1. B. Razavi, RF Microelectronics, 2nd Edition, Prentice-Hall, 1998.
2. Bosco H Leung, VLSI for Wireless Communication, Pearson Education, 2002.
3. Thomas H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 2003.
4. Emad N Farag and Mohamed I Elmasry, Mixed Signal VLSI Wireless Design Circuits and Systems, Kluwer Academic Publishers, 2000.
5. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, CMOS Wireless Transceiver Design, Boston, Kluwer Academic Publishers, 1997.

Hyperlinks:

1. http://nptel.iitm.ac.in

VEENG 641

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