Master of Technology
(VLSI and Embedded Systems)

Regulations, Curriculum and Syllabus
(Non CBCS)

(with effect from academic year 2018-2019)
i) **Regulations for (Non – CBCS) M.Tech. (VLSI and Embedded Systems)**

Besides the Non - CBCS regulations specified by Pondicherry University in respect of engineering post graduate degree admission, evaluation and awarding degree, the following norms are applicable for this programme.

1. **Name of the Programme** : M.Tech. (VLSI and Embedded Systems)
2. **Nature of the Programme** : Regular, Coming under Engineering Department.
3. **Programme Duration** : Two years (Four Semesters). However, one can complete the programme within maximum of eight semesters.
4. **Eligibility Criteria** : Candidates for admission to the first semester of four semester M.Tech (VLSI and Embedded Systems) should have passed B.E / B.Tech in Electronics and communication Engineering / Computer Science and Engineering/ Information Technology / Electrical and Electronics Engineering/ Instrumentation and Control Engineering/ Bio Medical Engineering/ Electronics and Instrumentation Engineering and other related branches, through regular course of study from an AICTE approved institution or an examination of any University or authority accepted by the Pondicherry University as equivalent thereto, with at least 55% marks in the degree examination or equivalent CGPA.

   **Note:**
   i. Candidates belonging to SC/ST who have a mere pass in the qualifying examination are eligible (as per university norms).
   ii. There is no age limit for M.Tech programmes.
5. **Admission Criteria** : The admission policy for various M.Tech programmes will be decided by the respective institutes offering M.Tech programmes subject to conforming to the relevant regulations of the Pondicherry University.
6. **Intake** : As per the sanctioned strength to the Institute by the Pondicherry University.
7. **Teaching and Learning Methods** : Lectures, tutorials and seminars are the main methods of course delivery, which would be supplemented by individual practical work, project work, simulation assignment, seminars and industrial visits.
8. Structure of M.Tech Programme:

8.1 The M.Tech Programmes is of semester pattern with 16 weeks of instruction in a semester.

8.2 The programme of instruction for each stream of specialization will consist of:
   i. Core courses (Compulsory)
   ii. Electives
   iii. Laboratory
   iv. Online course
   v. Internship
   vi. Project work

8.3 Credits will be assigned to the courses based on the following general pattern:
   i. One credit for each lecture period
   ii. One credit for each tutorial period
   iii. One credit for Project literature survey
   iv. Two credits for practical course
   v. Two credits for Online course
   vi. Two credits for Internship
   vii. Twelve credits for Project work
   viii. One teaching period shall be of 60 minutes duration including 10 minutes for discussion and movement.

8.4 Regulations, curriculum and syllabus of the M.Tech programme shall have the approval of Board of Studies and other Boards /Committees / Councils, prescribed by the Pondicherry University. The curriculum should be so drawn up that the minimum number of credits and other requirements for the successful completion of the programme will be as given in Table 1.

Table 1: Curriculum Details of the Programme

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Description</th>
<th>Requirements M.Tech (Full-Time)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Number of Semesters</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>Min. No. of credits of the Programme</td>
<td>74</td>
</tr>
<tr>
<td>3</td>
<td>Max. No. of credits of the Programme</td>
<td>74</td>
</tr>
<tr>
<td>4</td>
<td>Min. Cumulative Grade Point Average for pass</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>Min. period of completion of the Programme</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>Max. period for completing the Programme</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>(consecutive Semesters)</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Number of core and elective courses</td>
<td>18</td>
</tr>
<tr>
<td>9</td>
<td>Online course</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>Laboratory</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>Project work (semesters)</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>Internship</td>
<td>1</td>
</tr>
</tbody>
</table>
8.5 A core course is a course that a student admitted to the M.Tech programme must successfully complete to receive the degree. A student must register for all the core courses listed in the curriculum.

8.6 Elective courses are required to be chosen from the courses offered by the department(s) in that particular semester from among the approved courses. A core course of one department may be chosen as an elective by a student from other department***.

***Note: A candidate should successfully complete 7 electives for the award of degree. However, it is mandatory that the electives for each semester should be from the group of electives listed in curriculum.

8.7 Project work is envisaged to train a student to analyze independently any problem posed to him/her. The work may be analytical, experimental, design or a combination of both. The project report is expected to exhibit clarity of thought and expression.

8.8 The medium of instruction, examination, seminar and project work will be in English.

9. Requirements to appear for University Examination:

9.1 A candidate shall be permitted to appear for university examinations at the end of any semester only if he / she secures not less than 75% overall attendance arrived at by taking into account the total number of periods in all subjects put together offered by the institution for the semester under consideration. Candidates who secure overall attendance greater than 60% and less than 75% have to pay a condonation fee as prescribed by the University along with a medical certificate obtained from a medical officer not below the rank of Assistant Director to become eligible to appear for the examinations.

9.2 His / Her conduct should be satisfactory as certified by the Head of the institution.

10. Evaluation:

10.1 Theory Courses: 40% of marks for internal and 60% for end semester examinations.

The end semester question paper will have Part A (6 × 2 = 12 Marks) consisting of six two mark questions and Part B (4 × 12 = 48 Marks) consisting of six twelve mark descriptive questions of which one of them is compulsory and totally a candidate has to answer four out of six. For the end semester examination (University Semester Examination), the questions will be chosen only from the first four units of every theory subject of the programme to account end semester marks of 60 and internally (cumulatively) to assess a candidate’s depth of knowledge in the concerned subject for 40 marks, a minimum of two internal tests (30 marks) shall be conducted. Further, the content of the fifth unit in each subject shall be considered to conduct seminars, tutorials, simulations, assignments, development of hardware models etc. for 10 marks as it is formulated at system level for all subjects of the programme. The question paper setter will be appointed by the Competent Authority of the University. However, the evaluation shall be a central evaluation that shall be carried out by Controller of Examinations, Pondicherry University.
10.2 Practical Courses: 50% of marks for internal and 50% for the end semester examinations.

10.3 Internship / Seminar / Workshop / Conference / FDP / Short term course / NPTEL/GIAN/MOOC Course: 100% of marks through internal assessment only.

It is optional to undergo internship in established industry or esteemed institution / Seminar / Workshop / Conference / FDP / Short term course / NPTEL/GIAN/MOOC Course for a period of four weeks (20 working days) either in single or multiple spans by a candidate. Further, a presentation should be given regarding the training or programme underwent during the period with the submission of a report. There shall not be any end semester evaluation. However, the internal evaluation is done by the committee comprising of internal members and one external member from other department of the same institute constituted by Head of the Department for the award of appropriate grade to the candidate based on the performance. The distribution of marks will be decided by the committee. The internship / Seminar / Workshop / Conference / FDP / Short term course / NPTEL/GIAN/MOOC Course can be completed at any period of the duration of M.Tech. programme to fulfill the partial requirements for the award of M.Tech. degree.

10.4 NPTEL/GIAN/MOOC Course:

It is mandatory to undergo one course related to the chosen programme for the minimum period of 30 hours either from NPTEL or GIAN or MOOC that is to be completed at any period of the duration of M.Tech. programme to fulfill the partial requirements for the award of M.Tech. degree. Absolute grade shall be awarded to a candidate based on the marks given in the certificate issued by the competent authority (NPTEL or GIAN or MOOC) for the chosen course.

10.5 Project - Literature Survey:

100% of marks through internal assessment only. It is mandatory to undergo a complete literature survey by a candidate on the area of project work in the third semester regularly. There will be two reviews for the candidate on the literature survey carried out. There shall not be any end semester evaluation. However, the internal evaluation is based on the presentation of the candidate with the submission of a report about the literature survey. It will be done by the committee comprising of internal members and one external member from other department of the same institute constituted by Head of the Department for the award of appropriate grade to the candidate based on the performance. The distribution of marks for the literature survey will be decided by the committee.

10.6 Project and Viva Voce: 50% of marks for internal and 50% for end semester examinations.

The Project work shall be evaluated for a maximum of 100 marks. There shall be three assessments during the fourth semester by a review committee. The Head of the Department shall constitute the review committee consisting of supervisor, project coordinator and another faculty member from the Department for the internal
assessment (30 marks). The contribution by the respective supervisor of a student for 20 marks shall be accounted for the internal marks of 50. The end semester Project Viva Voce (for 50 marks) shall be conducted by the external member nominated by the competent Authority of the University. The distribution of the marks is shown in the Table given below.

Table 2: Allocation of marks

<table>
<thead>
<tr>
<th>Allocation of Marks for Project and Viva Voce (100 Marks)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Internal (50 Marks)</strong></td>
</tr>
<tr>
<td>Review Committee</td>
</tr>
<tr>
<td>Supervisor</td>
</tr>
<tr>
<td>Total</td>
</tr>
<tr>
<td>First Review</td>
</tr>
<tr>
<td>Second Review</td>
</tr>
<tr>
<td>Third Review</td>
</tr>
<tr>
<td>Marks</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>20 Marks</td>
</tr>
<tr>
<td>50 Marks</td>
</tr>
<tr>
<td>100 Marks</td>
</tr>
</tbody>
</table>

10.7 Publication: Mandatory requirement for the completion of the programme.

It is mandatory to have a minimum of one submitted manuscript / accepted publication in reputed journal during the M.Tech. programme. However, the submitted manuscript / accepted paper is subject to the recommendation of the evaluating committee comprising of internal members from same Department constituted by Head of the Department and one external member (examiner) from other institute nominated by competent Authority of University for the acceptance of the quality of the manuscript /paper of the candidate. The publication can be made at any period of the duration of M.Tech. programme. However, it does not contribute any credits to the programme but mandatory to fulfill the partial requirements for the award of M.Tech. degree. This evaluation process may be carried out along with even end semester examination depending up on the status of the students.

10.8 The end-semester examination shall be conducted by the Pondicherry University for all the courses offered by the department. A model question paper, as approved by the Chairperson, BOS (ECE), Pondicherry University, for each course offered under the curriculum should be submitted to the University.

10.9 The University shall adopt the double valuation procedure for evaluating the end-semester examinations, grading and publication of the results. Each answer script shall be evaluated by two experts. If the difference between the total marks awarded by the two examiners is not more than 15% of end-semester examination maximum marks, then the average of the total marks awarded by the two examiners will be reckoned as the mark secured by the candidate; otherwise, a third examiner is to be invited to evaluate the answer scripts and his/her assessment shall be declared final.

10.10 Continuous assessment of students for theory courses shall be based on two tests (15 marks each) and one assignment (10 marks). A laboratory course carries an internal assessment mark of 50 distributed as follows: (i) Regular laboratory exercises and records – 20 marks (ii) Internal laboratory test – 20 marks and (iii) Internal viva-voce – 10 marks.
10.11 All eligible students shall appear for the University examination.

11. Grading

11.1 The assessment of a course will be done on absolute marks basis. However, for the purpose of reporting the performance of a candidate, letter grades, each carrying stipulated points, will be awarded as per the range of total marks (out of 100) obtained by the candidate, as detailed below in Table 3.

Table 3: Letter Grade and the Corresponding Grade Point

<table>
<thead>
<tr>
<th>Range of Total Marks</th>
<th>Letter Grade</th>
<th>Grade Point</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 to 100</td>
<td>S</td>
<td>10</td>
<td>Excellent</td>
</tr>
<tr>
<td>80 to 89</td>
<td>A</td>
<td>9</td>
<td>Very Good</td>
</tr>
<tr>
<td>70 to 79</td>
<td>B</td>
<td>8</td>
<td>Good</td>
</tr>
<tr>
<td>60 to 69</td>
<td>C</td>
<td>7</td>
<td>Above Average</td>
</tr>
<tr>
<td>55 to 59</td>
<td>D</td>
<td>6</td>
<td>Average</td>
</tr>
<tr>
<td>50 to 54</td>
<td>E</td>
<td>5</td>
<td>Satisfactory</td>
</tr>
<tr>
<td>0 to 49</td>
<td>F</td>
<td>0</td>
<td>Failure</td>
</tr>
<tr>
<td>-</td>
<td>FA</td>
<td>-</td>
<td>Failure due to lack of attendance</td>
</tr>
<tr>
<td>-</td>
<td>AB</td>
<td>-</td>
<td>Failure by absence</td>
</tr>
</tbody>
</table>

11.2 A student is deemed to have completed a course successfully and earned the appropriate credit if and only if, he/she receives a grade of E or above. The student should obtain 40% of marks in the University examination in a subject to earn a successful grade.

A candidate shall be declared to have passed the examination in a subject of study only if he/she secures not less than 50% of the total marks (Internal assessment plus university examination marks).

11.3 A candidate who has been declared “Failed” in a course may reappear for that subject during the subsequent semester and secure a pass.

11.4 The internal assessment marks secured by a student in a theory course shall be considered only during the first appearance. For the subsequent attempts, the marks secured by the student in the University examination shall be scaled up to the total marks. Further, the marks secured by the student in the University examination in the latest attempt shall alone remain valid in total suppression of the University examination marks secured by the student in earlier attempts.
12. Declaration of Results, Rank and Issue of Grade Card

12.1 The results will be declared and the grade cards will be issued to the students after completing the valuation process.

12.2 The grade cards will contain the following details:

i. The college in which the candidate is studying/has studied.

ii. The list of courses enrolled during the semester and the grades scored.

iii. The Grade Point Average (GPA) for the semester and the Cumulative Grade Point Average (CGPA) of all enrolled subjects from first semester onwards.

12.3 GPA is the ratio of the sum of the products of the number of Credits (C) of courses registered and the corresponding Grade Point (GP) scored in those courses, taken for all the courses and the sum of number of credits of all the courses

\[
\text{GPA} = \frac{\text{Sum of } (C \times GP)}{\text{Sum of C}}
\]

The sum will cover all the courses the student has taken in that semester, including those in which he/she has secured F.

12.4 CGPA will be calculated in a similar manner, considering all the courses enrolled from first semester. FA grades are to be excluded for calculating GPA and CGPA. If a student has passed in a course after failing in earlier attempts, the grade secured by the student in the successful attempt only will be taken into account for computing CGPA.

12.5 To convert CGPA into percentage marks, the following formula shall be used:

\[
\% \text{ Mark} = (\text{CGPA} - 0.5) \times 10
\]

12.6 A candidate who satisfies the course requirements for all semesters and passes all the examinations prescribed for all the four semesters within a maximum period of eight (8) semesters reckoned from the commencement of the first semester to which the candidate was admitted, shall be declared to have qualified for the award of degree.

12.7 A candidate who qualifies for the award of the degree shall be declared to have passed the examination in FIRST CLASS with DISTINCTION upon fulfilling the following requirements:

i. Should have passed all the subjects pertaining to semesters 1 to 4 in his/her first appearance in 4 consecutive semesters starting from first semester to which the candidate was admitted.

ii. Should not have been prevented from writing examinations due to lack of attendance.

iii. Should have secured a CGPA of 8.50 and above from semesters 1 to 4.

12.8 A candidate who qualifies for the award of the degree by passing all the subjects relating to semesters 1 to 4 and secure
CGPA not less than 6.5 shall be declared to have passed the examination in FIRST CLASS. All other candidates who qualify for the award of degree shall be declared to have passed the examination in SECOND CLASS.

12.9 A student with CGPA less than 5.0 is not eligible for the award of degree.

12.10 For the award of University rank and gold medal, the CGPA secured from 1st to 4th semester should be considered and it is mandatory that the candidate should have passed all the subjects from 1st to 4th semester in the first appearance and he/she should not have been prevented from writing the examination due to lack of attendance and should not have withdrawn from writing the University examinations.

13. Provision for Withdrawal : A candidate may, for valid reasons, and on the recommendation of the Head of the Institution be granted permission by the University to withdraw from writing the entire semester examination as one UNIT. The withdrawal application shall be valid only if it is made earlier than the commencement of the last theory examination pertaining to that semester. Withdrawal shall be permitted only once during the entire programme. Other conditions being satisfactory, candidates who withdraw are also eligible to be awarded DISTINCTION whereas they are not eligible to be awarded a rank/gold medal.

14. Temporary Discontinuation from the Programme : If a candidate wishes to temporarily discontinue the programme for valid reasons, he/she shall apply through the Head of the Institution in advance and obtain a written order from the University permitting discontinuance. A candidate after temporary discontinuance may rejoin the programme only at the commencement of the semester at which he/she discontinued, provided he/she pays the prescribed fees to the University. The total period of completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not in any case exceed 4 years, including the period of discontinuance.

15. Revision of Regulations and Curriculum : The University may from time to time revise, amend or change the regulations of curriculum and syllabus as and when requirement for the same arises.

16. Power to Modify : 15.1 Notwithstanding anything contained in the foregoing, the Pondicherry University shall have the power to issue directions/orders to remove any difficulty.

15.2 Nothing in the foregoing may be construed as limiting the power of the Pondicherry University to amend, modify or repeal any or all of the above.

17. Minimum number of credits to be acquired for successful completion of the programme : 74 (Seventy Four) Credits
### ii) Curriculum of M.Tech. (VLSI and Embedded Systems)

#### I Semester

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course Code</th>
<th>Name of the Course</th>
<th>H/S</th>
<th>L-T-P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VEENG 510</td>
<td>VLSI Design Laboratory</td>
<td>H</td>
<td>0-0-4</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>VEENG 511</td>
<td>Applied Mathematics</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>VEENG 512</td>
<td>Digital System Design</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>VEENG 513</td>
<td>Microcontroller Based System Design</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>VEENG 514</td>
<td>VLSI Design Techniques</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>Elective I</td>
<td></td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>Elective II</td>
<td></td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total Credits for Semester I</strong></td>
<td></td>
<td></td>
<td><strong>24</strong></td>
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</table>

(H – Hard Core Course; S – Soft Core Course)

#### II Semester

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course Code</th>
<th>Name of the Course</th>
<th>H/S</th>
<th>L-T-P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>VEENG 520</td>
<td>Embedded System Design Laboratory</td>
<td>H</td>
<td>0-0-4</td>
<td>2</td>
</tr>
<tr>
<td>9</td>
<td>VEENG 521</td>
<td>Advanced Digital System Design</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>VEENG 522</td>
<td>Embedded Networking</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>11</td>
<td>VEENG 523</td>
<td>Embedded System Design</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>12</td>
<td>VEENG 524</td>
<td>Low Power Digital VLSI Design</td>
<td>H</td>
<td>3-1-0</td>
<td>4</td>
</tr>
<tr>
<td>13</td>
<td>Elective III</td>
<td></td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>Elective IV</td>
<td></td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total Credits for Semester II</strong></td>
<td></td>
<td></td>
<td><strong>24</strong></td>
</tr>
</tbody>
</table>

(H – Hard Core Course; S – Soft Core Course)
### III Semester

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course Code</th>
<th>Name of the Course</th>
<th>H/S</th>
<th>L-T-P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>15.</td>
<td></td>
<td>Elective V</td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>16.</td>
<td></td>
<td>Elective VI</td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>17.</td>
<td></td>
<td>Elective VII</td>
<td>S</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>18.</td>
<td>VEENG 610</td>
<td>Internship/ Seminar/ Workshop / Conference / FDP / Short Term Course / NPTEL/GIAN/MOOC Course</td>
<td>H</td>
<td>0-0-2</td>
<td>2</td>
</tr>
<tr>
<td>19.</td>
<td>VEENG 611</td>
<td>NPTEL/GIAN/MOOC Course</td>
<td>H</td>
<td>0-2-0</td>
<td>2</td>
</tr>
<tr>
<td>20.</td>
<td>VEENG 612</td>
<td>Project – Literature Survey</td>
<td>H</td>
<td>0-0-1</td>
<td>1</td>
</tr>
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</table>

**Total Credits for Semester III** 14

(H – Hard Core Course; S – Soft Core Course)

### IV Semester

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course Code</th>
<th>Name of the Course</th>
<th>H/S</th>
<th>L-T-P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>21.</td>
<td>VEENG 620</td>
<td>Project and Viva Voce</td>
<td>H</td>
<td>0-0-12</td>
<td>12</td>
</tr>
<tr>
<td>22.</td>
<td>VEENG 621</td>
<td>Publication</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
</tbody>
</table>

**Total Credits for Semester IV** 12

(H – Hard Core Course; S – Soft Core Course)

Total number of credits required to complete M.Tech in VLSI and Embedded Systems: 74 credits
### Semester I – List of Electives

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Course Code</th>
<th>Name of the Course</th>
<th>L-T-P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>VEENG 530</td>
<td>Embedded Technology</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>2.</td>
<td>VEENG 531</td>
<td>FPGA based System Design</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>3.</td>
<td>VEENG 532</td>
<td>Modeling and Synthesis with Verilog HDL</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>4.</td>
<td>VEENG 533</td>
<td>Physical Design of VLSI</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>5.</td>
<td>VEENG 534</td>
<td>Real Time Operating System</td>
<td>2-1-0</td>
<td>3</td>
</tr>
<tr>
<td>6.</td>
<td>VEENG 535</td>
<td>Soft Computing</td>
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<td>Software for Embedded System</td>
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<td>8.</td>
<td>VEENG 537</td>
<td>VLSI Architecture</td>
<td>2-1-0</td>
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### Semester II - List of Electives

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<tr>
<th>Sl. No.</th>
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<tr>
<td>1.</td>
<td>VEENG 550</td>
<td>DSP Processor Architecture and Programming</td>
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<td>2.</td>
<td>VEENG 551</td>
<td>Embedded Control System</td>
<td>2-1-0</td>
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<td>VEENG 552</td>
<td>High Speed Digital Design</td>
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<td>VEENG 553</td>
<td>Principles of ASIC Design</td>
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<td>VEENG 554</td>
<td>Real Time Systems</td>
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<td>VEENG 555</td>
<td>RISC Processor Architecture and Programming</td>
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<td>VEENG 556</td>
<td>Testing of VLSI Circuits</td>
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<tr>
<td>1.</td>
<td>VEENG 630</td>
<td>Advanced Embedded System</td>
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<td>VEENG 631</td>
<td>Advanced Image Processing</td>
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<td>VEENG 632</td>
<td>CAD for VLSI Circuits</td>
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<td>Design of Analog and Mixed VLSI Circuits</td>
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<td>VEENG 634</td>
<td>Distributed Embedded Computing</td>
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<td>Hardware Software Co-Design</td>
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<td>Micro-Electromechanical Systems</td>
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<td>VEENG 637</td>
<td>Nano Electronics</td>
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<td>VEENG 638</td>
<td>Pervasive Devices and Technology</td>
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<td>VEENG 639</td>
<td>Robotics and Automation</td>
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<td>VEENG 640</td>
<td>System-on-Chip Design</td>
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<td>12.</td>
<td>VEENG 641</td>
<td>VLSI for Wireless Communication</td>
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iii) **Syllabus for M.Tech. (VLSI and Embedded Systems):**

<table>
<thead>
<tr>
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<tr>
<td>VEENG 510</td>
<td>VLSI DESIGN LAB</td>
<td>L 0</td>
<td>T 0</td>
<td>P 4</td>
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</table>

**Objective:** Hands on experience on various simulation tools to design and analyze the combinational and sequential circuits.

**LIST OF EXPERIMENTS:**
(Given the list is minimal, however, the course teacher can decide the level of experiments)

1. Design and simulate combinational circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
   a. Adder, subtractor circuits
   b. Code converter circuits
   c. Decoder circuit
   d. Encoder circuit
   e. Multiplexer
   f. Demultiplexer
   g. Parallel adder/subtractor
   h. Multiplier
   i. Divider

2. Design and simulate sequential circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
   a. Flip-flops
   b. Shift registers (SISO, SIPO, PISO, PIPO)
   c. Synchronous counter
   d. Asynchronous counter
   e. Mod counter
   f. Sequence generator
   g. Sequence detector
   h. Ring and Johnson counter

3. Simulation of NMOS and CMOS circuits using SPICE.

4. FPGA/CPLD real time programming and I/O interfacing.

5. Implementation of combinational circuit in FPGA/CPLD

6. Implementation of sequential circuit in FPGA/CPLD

**VEENG 510**
Prerequisite: Knowledge in Graph theory and Boolean functions.

Objective: To learn the Boolean functions, Graphical and Optimization techniques in the design and analysis of systems.

Outcome: The students will understand the different concepts of Graphs, Boolean algebra and Operation Research and will be able to solve problems in the engineering field.

Unit I: Basics of Graph Theory 12 Hours

Unit II: Graph Algorithm 12 Hours
Computer Representation of graphs: Basic graph algorithms - Minimal spanning tree algorithm - Kruskal and Prim’s algorithm - Shortest path algorithms - Dijsktra's algorithm - DFS and BFS algorithms; Lattices as partially ordered sets: properties of Lattices. Lattices as Algebraic Systems-Sublattices

Unit III: Boolean Algebra 12 Hours
Definitions and examples: Subalgebra - Direct Product and Homomorphism-Boolean Functions-Representation and Minimization of Boolean Functions- Design examples using Boolean Algebra.

Unit IV: Optimization Techniques 12 Hours
Linear Programming: Formulation of LPP - Graphical methods - Simplex method- Transportation problems- Assignment problems.

Unit V: Instructional Activities 12 Hours
Applications of Boolean Functions - Practical applications of Basic graph algorithms, Transportation problems and Assignment problems.
Reference Books:
2. Narsingh Deo, Graph Theory: With Application to Engineering and Computer Science, PHI, 2014.

Hyperlinks:
1. http://www.nptel.ac.in

VEENG 511
<table>
<thead>
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<td>VEENG 512</td>
<td>DIGITAL SYSTEM DESIGN</td>
<td>L 3 T 1 P 0</td>
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**Prerequisite:** Basics of Electronics and Programming

**Objective:** To expose the students in the fundamentals of combinational and sequential circuits and study the concepts of VHDL for digital circuits.

**Outcome:** Design and analyze combinational and sequential circuits using VHDL code.

**Unit I: Digital Systems Overview**
12 Hours

**Unit II: Hardware Description Language**
12 Hours

**Unit III: Design of Networks for Arithmetic Operations**
12 Hours
Design of Parallel adder/subtractor with accumulator : Serial adder with accumulator- design of binary multiplier and binary divider- signed multiplier using VHDL.

**Unit IV: Designing with Programmable Logic Devices**
12 Hours
Read Only Memories: Programmable Array Logic PALs- Programmable Logic Arrays PLAs - PLA minimization and PLA folding; Other Sequential PLDs- Design of combinational circuits using PLD’s.

**Unit V: Instructional Activities**
12 Hours
Simulation of logic gates- adder- subtractor- decoder-multiplexer-flip flops- counters using VHDL.
Reference Books:

Hyperlinks:
1. http://www2.cs.uidaho.edu/~krings/CS449

VEENG 512
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<td>VEENG 513</td>
<td>MICROCONTROLLER BASED SYSTEM DESIGN</td>
<td>L T P 3 1 0</td>
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</table>

**Prerequisite**: Knowledge in Digital Electronics, Architecture and programming in Microprocessors

**Objective**: To impart knowledge on Microcontroller based system design and its application

**Outcome**: Able to understand and analyze the Microcontroller Architecture and peripherals with its application

**Unit I**: 8051 Architecture 12 Hours

**Unit II**: Programming 12 Hours
Assembly language programming: Arithmetic Instructions - Logical Instructions - Single bit Instructions - Timer Counter Programming - Serial Communication Programming - Interrupt Programming; RTOS for 8051: RTOS Lite - Full RTOS - Task creation and run - LCD digital Clock/thermometer using Full RTOS

**Unit III**: PIC Microcontroller 12 Hours
Architecture: Memory organization - Addressing modes - Instruction set - PIC programming in Assembly & C - I/O port - Data Conversion - RAM & ROM Allocation - Timer programming.

**Unit IV**: Peripheral of PIC Microcontroller 12 Hours

**Unit V**: Instructional Activities 12 Hours
Microcontroller based system design: Interfacing LCD Display - Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control - Controlling DC/ AC appliances - Measurement of frequency - Stand alone Data Acquisition System.
**Reference Books:**


**Hyperlinks:**

1. http://www.nptel.iitm.ac.in
2. http://www.microchip.com/design-centers/microcontrollers
3. https://learn.mikroe.com/

VEENG 513
<table>
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<td>VEENG 514</td>
<td>VLSI DESIGN TECHNIQUES</td>
<td>L 3 T 1 P 0</td>
<td>4</td>
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</table>

**Prerequisite**: Basic concepts in Digital Circuit Design

**Objective**: To understand the design and analysis of digital VLSI chips using CMOS technology

**Outcome**: Can understand the design issues at the layout, transistor logic and register-transfer level.

**Unit I**: MOS transistor theory and process technology 12 hours

NMOS and PMOS transistors: Threshold voltage - Body effect- Design equations - Second order effects. MOS models and small signal AC characteristics- Basic CMOS technology.

**Unit II**: Inverters and Logic gates 12 hours

NMOS and CMOS Inverters: Stick diagram- Inverter ratio- DC and transient characteristics - switching times- Super buffers- Driving large capacitance loads; CMOS logic structures: Transmission gates- Static CMOS design- Dynamic CMOS design.

**Unit III**: Circuit characterization and Performance estimation 12 hours


**Unit IV**: VLSI system components, circuits and design 12 hours

Multiplexers - Decoders – comparators - priority encoders - Shift registers - Arithmetic circuits: Ripple carry adders- Carry look ahead adders- High-speed adders; Multipliers. Physical design - Delay modeling - cross talk - floor planning - power distribution - Clock distribution; Basics of CMOS testing.

**Unit V**: Instructional Activities 12 Hours

Case study on Overview of digital design with Verilog HDL for Structural - Data flow - Behavioral Styles of Hardware Description
Reference Books:

Hyperlinks:
1. http://web.ewu.edu
2. http://ic.sjtu.edu

VEENG 514
Objective: Hands on experience to design various applications for microcontroller based system design in order to acquire sufficient knowledge and to understand embedded system design based applications.

LIST OF EXPERIMENTS:
(Given the list is minimal, however, the course teacher can decide the level of experiments)

1. Interfacing the microcontroller to a PC through RS232 and displaying the messages sent by the microcontroller on the PC.

2. Design With PIC and Arduino Microcontrollers - Assembly or C Programming/Arduino IDE programming to interface
   a. 7 segment displays to display the measured voltage from 0 to 5 volts
   b. LDR to display light intensity in 7 segment display
   c. Temperature sensor to display temperature in 7 segment display
   d. Pressure sensor to display measured pressure in 7 segment display
   e. PH sensor to display measured value in 7 segment display
   f. Ultrasonic sensor to display distance in 7 segment display
   g. Noise sensor to display noise level in 7 segment display

3. Interface DC motor with Microcontroller and control its speed and direction using PWM

4. Microcontroller based system design
   a. Lamp controller using a light sensor and a timer
   b. Water Pump Controller to maintain water level in a tank
   c. Moisture controller using moisture and sprinkler controller

5. Design Real time clock

6. Wireless data transfer using Microcontroller

7. Color identification and tracking using Raspberry pi

VEENG 520
Course Code | Name of the Course | Periods | Credits | Total Hours
---|---|---|---|---
VEENG 521 | ADVANCED DIGITAL SYSTEM DESIGN | L T P | 4 | 60

**Prerequisite**: Knowledge on digital integrated circuit design, Verilog and FPGA.

**Objective**: To make the students to understand the design and analysis of the synchronous and asynchronous sequential circuits.

**Outcome**: The students will be able to design sequential circuits and fault diagnosis algorithms.

**Unit I: Sequential Circuit Design**
12 Hours
Analysis of clocked synchronous sequential circuits and modeling: state diagram - state table - state table assignment and reduction - design of iterative circuits - ASM chart and realization using ASM.

**Unit II: Asynchronous Sequential Circuit Design**
12 Hours

**Unit III: Synchronous Design Using Programmable Devices**
12 Hours
Programming logic device families: Designing a synchronous sequential circuit using PLA/PAL - realization of finite state machine using PLD/FPGA.

**Unit IV: Fault Diagnosis And Testability Algorithms**
12 Hours

**Unit V: Instructional Activities**
12 Hours
Simulation of synchronous/ asynchronous sequential circuits: Logic compilation - two level and multi level logic synthesis - sequential logic synthesis - technology mapping - tools for mapping to PLDs and FPGAs.
Reference books:

Hyperlinks:

VEENG 521
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<tr>
<td>VEENG 522</td>
<td>EMBEDDED NETWORKING</td>
<td>L</td>
<td>T</td>
<td>P</td>
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</tbody>
</table>

**Prerequisite:** Basic knowledge in Microcontrollers

**Objective:** To impart knowledge on communication protocols, USB and CAN bus Embedded Ethernet

**Outcome:** Design and development of Serial and parallel communication, USB and CAN bus for Embedded networking

**Unit I: Embedded Communication Protocols**
12 hours

Embedded Networking: Introduction - Serial/Parallel Communication - Serial communication protocols - RS232 standard - RS485 - Synchronous Serial Protocols - Serial Peripheral Interface (SPI) - Inter Integrated Circuits (I²C) - PC Parallel port programming - ISA/PCI Bus protocols - Fire wire

**Unit II: USB and CAN bus**
12 hours


**Unit III: Ethernet Basics**
12 hours


**Unit IV: Embedded Ethernet**
12 hours

Exchanging messages using UDP and TCP - Serving web pages with Dynamic Data - Serving web pages that respond to user Input - Email for Embedded Systems - Using FTP - Keeping Devices and Network secure.

**Unit V: Instructional Activities**
12 Hours

Serial and parallel protocols used in industries – its timing diagram, Serial communication with an Arduino, visualize the Ethernet traffic using protocol analyzer.
**Reference Books:**


**Hyperlink:**

1. http://www.nptel.iitm.ac.in

**VEENG 522**
**Course Code** | **Name of the Course** | **Periods** | **Credits** | **Total Hours**
---|---|---|---|---
VEENG 523 | EMBEDDED SYSTEM DESIGN | L T P | 4 | 60

**Prerequisite:** Basic Knowledge in Digital Electronics and microcontroller

**Objective:** To understand basic concepts, Building Blocks for Embedded System development

**Outcome:** Design real time embedded systems using the concepts of RTOS and ability to understand the role of embedded systems in industry

**Unit I: Introduction**

Embedded system overview, Design challenge: Optimizing design metrics- Processor Technology- General purpose Processors- Single purpose Processors and Application Specific Processors; IC Technology: Full custom/VLSI, Semicustom ASIC- PLD- Trends- Design Technology

**Unit II : Custom Single purpose Processor**

RTL combinational components: RTL sequential components - Custom Single purpose Processor Design- RTL Custom Single purpose Processor Design- Optimizing Custom Single purpose Processors- Optimizing the original program- Optimizing the FSMD- Optimizing the data path-optimizing the FSM

**Unit III : General purpose Processors**

Basic architecture: Data path- Control Unit - Memory - Instruction execution and Pipelining; Superscalar and VLIW architectures- Application Specific Instruction set Processors (ASIP’s), Microcontrollers- DSP- Less General ASIP environments- Selecting a Microprocessor and General purpose processor design.

**Unit IV : Embedded OS**

Creating embedded operating system: Basis of a simple embedded OS - Introduction to sEOS - Using Timer 0 and Timer 1- Portability issue-Alternative system architecture- Important design considerations when using sEOS.

**Unit V: Instructional Activities**

Reference Books:


Hyperlinks:

1. http://www.nptel.ac.in/courses/117106030/35

VEENG 523
Prerequisite: Fundamentals of VLSI design.

Objective: To discuss low power design methodologies at various design levels from the circuit level to the system level and also power estimation with optimization techniques.

Outcome: Students will be able to design low power VLSI circuits.

Unit I: Power Dissipation 12 hours
Introduction: Need for low power circuit design - sources of power consumption - design methodology - low power figure of merits - limits and applications of low power VLSI Design

Unit II: Power Analysis 12 hours
Power Analysis: SPICE circuit simulation - discrete transistor modeling and analysis - gate level 0 logic simulation - architecture level analysis - data correlation analysis; Probabilistic Power Analysis: Random logic signals - probabilistic power analysis techniques - signal entropy.

Unit III: Circuit and Logic Level 12 hours
Circuit Level: Transistor and gate sizing - equivalent pin ordering - network restructuring and reorganization - special latches and flip flops; Logic Level: Gate reorganization - signal gating - logic encoding - precipitation logic.

Unit IV: Energy Recovery Techniques 12 hours

Unit V: Instructional Activities 12 Hours
Simulation Study: Sources of power dissipation in SRAMs - Low power SRAM circuit techniques; Sources of power dissipation in DRAMs - Low power DRAM circuit techniques using related tools.
Reference Books:

Hyperlinks:
1. http://www.nptel.iitm.ac.in/courses/106105034/

VEENG 524
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<td>VEENG 530</td>
<td>EMBEDDED TECHNOLOGY</td>
<td>L 2 T 1 P 0</td>
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**Prerequisite**: Basic Knowledge in communication networks

**Objective**: To study the basics of OSI reference model and introduce multiboard communication software.

**Outcome**: Understand the concept of switches and routers for protocol implementation and design the communication protocol for multiboard

**Unit I: OSI Reference Model**
- Communication Devices
- Communication Echo System
- Design Consideration
- Host Based Communication
- Embedded Communication System
- OS Vs RTOS

**9 Hours**

**Unit II: Software Partitioning**
- Limitation of strict Layering
- Tasks & Modules
- Modules and Task Decomposition
- Layer2 Switch
- Layer3 Switch / Routers
- Protocol Implementation
- Management Types
- Debugging Protocols

**9 Hours**

**Unit III: Tables & Other Data Structures**
- Partitioning of Structures and Tables
- Implementation
- Speeding Up access
- Table Resizing
- Table access routines
- Buffer and Timer Management
- Third Party Protocol Libraries

**9 Hours**

**Unit IV: Management Software**
- Device Management
- Management Schemes
- Router Management
- Management of Sub System Architecture
- Device to manage configuration
- System Start up and configuration

**9 Hours**

**Unit V: Instructional Activities**
- Implementation of 7 layer OSI in CIM: A case study
- Connecting a classified network to the Internet
- Embedded Communication System
- An internet Routing and firewall security
- Simulation of Partitioning of Structures
- Simulation of Speeding Up access

**9 Hours**
Reference Books:

Hyperlinks:
2. ieeexplore.ieee.org/abstract/document/6976507
3. http://nptel.ac.in/courses/117106030/35
5. https://sans.org

VEENG 530
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<td>FPGA BASED SYSTEM DESIGN</td>
<td>L 2</td>
<td>T 1</td>
<td>P 0</td>
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**Prerequisite:** Knowledge on Digital system design and fundamentals of PLD

**Objective:** To provide in depth understanding of logic and system design, synthesis of advanced digital hardware systems in FPGA tools

**Outcome:** Design and model the digital circuits with HDL at behavioral, structural, and RTL Levels and implemented in FPGA

**Unit I: FPGA Architecture**  
9 Hours  
Introduction of basic concepts: Digital design and FPGAs- FPGA based system design- Logic blocks- Routing architecture- FPGA Fabrics- Circuit design of FPGA fabrics- Platform FPGA.

**Unit II: Technology mapping for FPGAs**  
9 Hours  

**Unit III: Routing for FPGAs**  
9 Hours  
Routing terminology - Strategy for routing in FPGAs -Routing for row-logic block selection- Experimental procedure Logic block architecture -Logic block functionality vs area and efficiency- Logic block selection- Experimental procedure-Logic block area and routing model.

**Unit IV: Architecture of FPGAs**  
9 Hours  
Study of Xilinx Virtex series FPGAs, Architecture of Altera cyclone FPGA series. Comparison of Xilinx & Altera FPGAs

**Unit V: Instructional Activities**  
9 Hours  
Synthesis of multiplier and digital filters in FPGA- Analyse the FPGA architecture and mapping of I/O pads
Reference Books:

Hyperlinks:
1. http://nptel.iitm.ac.in

VEENG 531
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<tr>
<td>VEENG 532</td>
<td>MODELLING AND SYNTHESIS WITH VERILOG HDL</td>
<td>L2 T1 P0</td>
<td>3</td>
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**Prerequisite:** Basic Knowledge in Digital Circuits And Hardware Modeling

**Objective:** To introduce the concepts of hardware modeling with Verilog HDL, synthesis of logic circuit and also study the electronic design automation in VLSI.

**Outcome:** Exposure in layout/design and design automation process.

**Unit - I: Hardware Modeling With Verilog HDL**

HDLs in EDA: System C, VHDL and Verilog- System Verilog overview- Hardware Encapsulation- Hardware Modeling with Verilog HDL- Hierarchical descriptions of hardware- Structured design methodology- Arrays, Using Verilog for synthesis- Event driven simulation and test benches- Logic system, data types and operators; User-defined primitives: Combinational behavior-Sequential behavior.

**Unit - II: Delay Models, Behavioral Description**

Verilog models of propagation delay: Built-in constructs- Inertial delay,- Time scales and precision- Delays- Delay effects and Pulse rejection- Race condition in Verilog- Types of race condition- Task and function- Events, Process control, Disable a block- Watchdog- debugging, Code coverage- Testing strategies- File handling- Behavioral descriptions in Verilog HDL

**Unit - III: Synthesis of Combinational Logic, Sequential Logic**


**Unit - IV: Synthesis of Language Constructs, Switch Level Models**

Synthesis of Language constructs: MOS Transistor Technology- Switch-Level Models- PULL gates- CMOS Transmission gates- Bi-Directional gates (Switches) - Signal Strengths- Strength Reduction by Primitives- Combination and Resolution of Signal Strengths- Signal Strengths and Wired Logic

**Unit - V: Instructional Activities**

References Books:
7. S-Edit v13.0 user guide by Tanner EDA tool.

Hyperlinks:
1. http://web.ewu.edu
2. http://nptel.iitm.ac.in

VEENG 532
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<td>VEENG 533</td>
<td>PHYSICAL DESIGN OF VLSI</td>
<td>L 2 T 1 P 0</td>
<td>3</td>
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</table>

**Prerequisite:** Basic concepts in digital circuit design

**Objective:** To introduce the physical design concepts such as routing, placement, partitioning and packaging

**Outcome:** The students will be able to understand the design concepts and circuit layouts

**Unit I: Introduction To VLSI Technology**

9 Hours


**Unit II: Placement Using Top-Down Approach**

9 Hours

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut-partition with capacity and i/o constraints; Floor planning: Rectangular dual floor planning-hierarchical approach-simulated annealing-Floor plan sizing; Placement: Cost function-force directed method-placement by simulated annealing-partitioning placement-module placement on a resistive network-regular placement-linear placement

**Unit III: Routing Using Top Down Approach**

9 Hours

Fundamentals: Maze running-line searching-Steiner trees; Global Routing: Sequential Approaches-hierarchical approaches-multi-commodity flow based techniques-Randomised Routing-One Step approach-Integer Linear Programming; Detailed Routing: Channel Routing-Switch box routing; Routing in FPGA: Array based FPGA-Row based FPGAs

**Unit IV: Performance Issues In Circuit Layout**

9 Hours


**Unit V: Instructional Activities**

9 Hours

Planar subset problem (PSP) - Single layer global routing-Single Layer Global Routing-Single Layer detailed Routing-Wire length and bend minimization technique-Over the Cell (OTC) Routing-Multiple chip modules (MCM) - Programmable Logic Arrays-Transistor chaining-Wein-Burger Arrays-Gate matrix layout-1D compaction-2D compaction
Reference Books:


Hyperlink:

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in

VEENG 533
VEENG 534  |  REAL TIME OPERATING SYSTEM  |  L  |  T  |  P  |  3  |  45  

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**Prerequisite**  
Basic knowledge in Computer Programming and microcontroller based system

**Objective**  
To expose the fundamentals of interaction of OS with a computer and application development using RTOS

**Outcome**  
To acquire knowledge in the basic concept of embedded system

**Unit I: Structure Of RTOS μCOS / Embedded Linux**  
9 Hours
- RTOS features: Resources and shared resources Task, Task control block- Task scheduling-Task level context switching- Syntax related to Context switching- Locking and unlocking of scheduler-Idle & Static task- Interrupt under RTOS- ISR under RTOS - Servicing an interrupt- Clock Tick.
- Initialization and Starting the RTOS- Multitasking- Task Management function- Event Control Blocks-Task State Management.

**Unit II: Synchronization & Communication in μCOS-II / Embedded Linux**  
9 Hours
- Semaphore management Functions with μCOS-II / Embedded Linux API - ECB as Semaphore, Mutual exclusion Semaphore functions- Event Flag management Functions- Mailbox management- ECB As Mailbox- Message Queue management- ECB as Message Queue- Message Queue Management Function

**Unit III: Process, I/O, Memory Management in RTOS**  
9 Hours
- Process Management- Timer functions- Device- File- I/O subsytems management- Memory Management- Memory Control Block- Dynamic memory allocation.

**Unit IV: WinCE**  
9 Hours

**Unit V: Instructional Activities**  
9 Hours
- Design and simulate static and dynamic scheduling algorithms in suitable platform- Study of RTOS used for Washing Machine- Air Conditioner- Microwave Oven- Engine Management System using CAN- Automatic Chocolate Vending Machine
Reference Books:

Hyperlinks:
1. http://www.nptel.iitm.ac.in

VEENG 534
**Course Code** | **Name of the Course** | **Periods** | **Credits** | **Total Hours**
---|---|---|---|---
VEENG 535 | SOFT COMPUTING | L T P | 3 | 45

**Prerequisite:** Fundamentals of VLSI design.

**Objective:** To discuss low power design methodologies at various design levels from the circuit level to the system level and also power estimation with optimization techniques.

**Outcome:** Students will be able to design low power VLSI circuits.

**Unit I: Neural Network**  
9 Hours  

**Unit II: Fuzzy Sets & Logic**  
9 Hours  

**Unit III: Genetic Algorithm**  
9 Hours  
Role of GA - fitness function - selection of initial population - cross over (different types) - mutation - inversion - deletion - constraints handling and applications of travelling salesman and graph coloring.

**Unit IV: Hybrid Systems**  
9 Hours  
Hybrid Systems: GA based BPNN (Weight determination) - Neuro fuzzy systems - Fuzzy BPNN - fuzzy neuron - architecture - learning - Fuzzy logic controlled genetic algorithm.

**Unit V: Instructional Activities**  
9 Hours  
Simulation of PSD - HSA and ACO related to either wireless networking or Antenna or Image Processing using related tools.
References Books:

Hyperlinks:

VEENG 535
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<td>VEENG 536</td>
<td>SOFTWARE FOR EMBEDDED SYSTEMS</td>
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Prerequisite: Basic Programming knowledge in C.

Objective: To introduce embedded software development process and Web enabling of systems.

Outcome: Gain knowledge and understanding of fundamental embedded systems design paradigms, architectures, possibilities and challenges, both with respect to software and hardware.

**Unit I: Programming Embedded Systems**
9 Hours

**Unit II: Python**
9 Hours

**Unit III: Embedded Program And Software Development Process**
9 Hours

**Unit IV: Unified Modeling Language**
9 Hours

**Unit V: Instructional Activities**
9 Hours
Reference Books:

Hyperlinks:
1. https://www.zapmeta.ws
2. http://nptel.ac.in/courses/117106030/35
3. https://link.springer.com

VEENG 536
Course Code | Name of the Course | Periods | Credits | Total Hours
---|---|---|---|---
VEENG 537 | VLSI ARCHITECTURE | L T P | 3 | 45

**Prerequisite**: Basic knowledge in logic circuit design

**Objective**: To introduce the features, programming and applications of programmable logic devices. Provide VLSI system design experience using FSM

**Outcome**: Students will be able to make the system level designs using FSM and analyze the performance with FPGA.

**Unit I: CMOS Design**
9 Hours
Overview of digital VLSI design Methodologies- Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- Layout diagram, Stick diagram-IC fabrications – Trends in IC technology.

**Unit II: Programmable Logic Devices**
9 Hours

**Unit III: Basic Construction, Floor Planning, Placement And Routing**
9 Hours

**Unit IV: Analog VLSI Design**
9 Hours

**Unit V: Instructional Activities**
9 Hours
Synthesis of the Ripple Carry Adder, Multiplier, Comparator, Shift registers and ALU circuits in CPLD devices and analyze the design with architecture.
Reference Books:

Hyperlinks:

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<td>DSP PROCESSOR ARCHITECTURE AND PROGRAMMING</td>
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**Prerequisite:** Basic Knowledge in processors, filter design and programming

**Objective:** To understand the techniques involved in real time DSP system and to design and implement a variety of algorithms for real world applications.

**Outcome:** Get familiar with the DSP processor architectures and practical knowledge with real time application.

**Unit I: Digital Signal Processing Systems**
9 Hours
Introduction to Digital signal processor architectures: Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

**Unit II: Digital Signal Processors**
9 Hours
TMS320C62x AND TMS320C64x: Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Real time implementations.

**Unit III: Implementation of Fast Fourier Transforms**
9 Hours
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

**Unit IV: FIR and IIR Filter Implementations**
9 Hours
FIR and IIR filters: Characteristics – Structures - FIR Filter design using Windowing and frequency sampling method - IIR Filter-Butterworth and Chebyshev Filter Design- Fixed point implementation using TMS320C64x - Floating point implementation using TMS320C67x.

**Unit V: Instructional Activities**
9 Hours
Simulate Auto Correlation and Cross correlation - Linear and circular Convolution- DFT/FFT, Design of FIR filter- Design of IIR filter
Reference Books:


Hyperlinks:

1. http://www.nptel.iitm.ac.in/courses
2. https://link.springer.com

VEENG 550
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<td>EMBEDDED CONTROL SYSTEM</td>
<td>L2 T1 P0</td>
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**Prerequisite**: Basic Knowledge in Micro controller

**Objective**: To expose the students to the fundamentals of Embedded System Blocks, fundamental RTOS and the Applications development

**Outcome**: Can understand and Design the embedded software for specific application

**Unit I: Embedded System Organization** 9 Hours

Embedded computing – characteristics of embedded computing applications – embedded system design challenges; Build process of Real time Embedded system – Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit –ISA, EISA bus;

**Unit II: Real-Time Operating System** 9 Hours

Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output – Non maskable interrupt, Software interrupt; Thread – Single, Multithread concept; Multitasking Semaphores.

**Unit III: Interface With Communication Protocol** 9 Hours

Design methodologies and tools – design flows – designing hardware and software Interface, – system integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming;

**Unit IV: Design Of Software For Embedded Control** 9 Hours

Software abstraction using Mealy-Moore FSM controller- Layered software development,-Basic concepts of developing device driver – SCI – Software - interfacing & porting using standard C & C++ ; Functional and performance Debugging with benchmarking Real-time system software

**Unit V: Instructional Activities** 9 Hours

Interface A/D & D/A converter- Design of Digital voltmeter- Interface PWM motor and control its speed, serial communication interface.
**References Books:**


**Hyperlinks:**

1. www.programmingembedded system.com
3. http://nptel.ac.in/courses/117106030/35

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<td>VEENG 552</td>
<td>HIGH SPEED DIGITAL DESIGN</td>
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**Prerequisite:** Basic knowledge in digital system design and electronics

**Objective:** To identify sources affecting the speed of digital circuits and to improve the signal transmission characteristics.

**Outcome:** Ability to identify sources affecting the speed of digital circuits and to improve the signal transmission characteristics.

**Unit I: Introduction**  
9 Hours
Frequency, time and distance - Capacitance and Inductance Effects - High speed properties of logical gates - Speed and power modeling of wires - Geometry and Electrical properties of wires - Electrical model of Transmission lines - Lossless LC transmission lines - Lossy RLC transmission lines - Special transmission lines.

**Unit II: Power Distribution and Noise**  
9 Hours
Power supply network - Local power regulation IR drops Area bonding - On chip bypass capacitors, Power supply isolation - Noise sources in digital system, Power supply Noise - Cross talk, Inter - symbol interference.

**Unit III: Signaling convention and Circuits**  
9 Hours
Signaling modes for transmission lines - Signaling over lumped transmission media, Signaling over RC interconnects, driving lossy LC lines- Terminators, transmitter and receiver circuits.

**Unit IV: Timing Convention and Synchronization**  
9 Hours

**Unit V: Instructional Activities**  
9 Hours
Study the characteristics of Transmission lines - Noise sources - ISI by simulation and measure ISI by CRO.
Reference Books:

Hyperlinks:
1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

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<td>VEENG 553</td>
<td>PRINCIPLES OF ASIC DESIGN</td>
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**Prerequisite**: Digital VLSI Design

**Objective**: To make the students to understand the architectural details of programmable ASICs including logic synthesis, floor-planning, placement and routing.

**Outcome**: The students will be able to gain sufficient theoretical knowledge for carrying out ASIC and FPGA design.

**Unit I: Introduction to Programmable Devices**
9 Hours
Programmable logic devices: ROM - PLA - PAL - PLD - FPGA - features, programming and applications using complex programmable logic devices; Speed performance and system programmability.

**Unit II: Introduction to ASIC**
9 Hours
Design flow - types of ASICs - full custom with ASIC - semi custom ASICs - standard cell based ASIC - gate array based ASIC - channeled - channel less - structured - data path elements - adders - multiplier - cell compilers; Logical effort: area and efficiency - paths - multi stage cells - optimum delay.

**Unit III: Low Level Design Language**
9 Hours
EDIF: PLA tools - introduction to CFI designs representation; Half gate ASIC: Introduction to synthesis and simulation - two level logic synthesis - high level logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

**Unit IV: Floor Planning, Placement and Routing**
9 Hours
Physical design: CAD tools - system partitioning - estimating ASIC size - partitioning methods; Floor planning tools - I/O and power planning - clock planning - placement algorithms - iterative placement improvement; Time driven placement methods - physical design flow global routing - local routing - detail routing - special routing - circuit extraction and DRC.

**Unit V: Instructional Activities**
9 Hours
Spartan 3E and Vertex Board Analysis - inputs and outputs - clock and power inputs - Xilinx I/O blocks - PLAs and PALs design using ASIC board.
Reference Books:

Hyperlink:
1. en.wikipedia.org/wiki/Standard_cell
2. www.utdallas.edu/~zhoud/DesignEntry
3. en.wikipedia.org/wiki/High-level_synthesis

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<td>REAL TIME SYSTEMS</td>
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Prerequisite: Basic Knowledge in Operating System and Microcontrollers

Objective: To provide the fundamental concepts in real time systems and basic multi-task scheduling algorithms

Outcome: Understand the concept of multi-task scheduling algorithms for various tasks as well as understand the impact of the latter two on scheduling

Unit I: Introduction

Unit II: Scheduling in Real-Time Systems
Scheduling of Dependent Tasks: Tasks with precedence relationships - Tasks sharing critical resources. Scheduling schemes for handling overload: Scheduling techniques in overload conditions - Handling real-time tasks with varying timing parameters - Handling overload conditions for hybrid task sets. Multiprocessor scheduling and comparison with uniprocessor scheduling.

Unit III: Programming Language And Tools

Unit IV: Real Time Databases
Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

Unit V: Instructional Activities
Study of operating System-Threads and Tasks-The Kernel, Time Services and Scheduling Mechanisms, other basic operating functions-Communication and Synchronization Application program interface and SSP structure.
Reference Books:

Hyperlinks:
1. nptel.ac.in/courses/106105036
2. http://www.slideshare.net/sanjivmalik/rtos-concepts

VEENG 554
Course Code  | Name of the Course                      | Periods | Credits | Total Hours |
-------------|----------------------------------------|---------|---------|-------------|
VEENG 555    | RISC PROCESSOR ARCHITECTURE AND PROGRAMMING | L T P   | 3       | 45          |

Prerequisite: Basic knowledge in Microprocessor and its Architecture

Objective: To introduce techniques for altering the existing processor architecture to suit recent developments.

Outcome: To analyze and develop RISC based architecture with protection techniques.

Unit I: AVR Microcontroller Architecture 9 Hours

Unit II: Peripheral Of AVR Microcontroller 9 Hours

Unit III: ARM Architecture and Programming 9 Hours

Unit IV: ARM Application Development 9 Hours

Unit V: Instructional Activities 9 Hours
Interfacing of various I/O devices and memory with ARM processor for home automation
Reference Books:

Hyperlinks:
1. http://www.nptel.iitm.ac.in

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<td>VEENG 556</td>
<td>TESTING OF VLSI CIRCUITS</td>
<td>L 2</td>
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**Prerequisite**: Basic knowledge in VLSI circuit design

**Objective**: To understand logic fault models and test generation for sequential and combinational logic circuits

**Outcome**: Gain more knowledge in the identification of faults in logic circuits with various fault models and various testing algorithms.

**Unit I: Testing and Fault Modelling**  
9 Hours

**Unit II: Test Generation**  
9 Hours
Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**Unit III: Design for Testability**  
9 Hours
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design.

**Unit IV: Self Test and Test algorithms**  
9 Hours

**Unit V: Instructional Activities**  
9 Hours
Reference Books:

Hyperlink:
1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in

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**Prerequisite:** Knowledge in Digital Signal Processing

**Objective:** To introduce techniques for signal processing based architecture to suit VLSI implementation.

**Outcome:** Gain knowledge in various architecture for VLSI signal processing

**Unit I: Parallel processing in FIR filter Realization**
9 Hours
DSP systems: Programs- Applications- Representation- Data flow graphs; Loop Bound and Iteration Bound- Algorithms- Iteration Bound of Multirate Data-flow graphs- Pipelining of FIR filters- Parallel Processing of FIR filters.

**Unit II: Systolic Architecture Design**
9 Hours

**Unit III: Efficient Realization of IIR filters in DSP**
9 Hours
Fast convolution algorithms: Iterated- Cyclic Convolutions- Design by Inspection- DCT and Inverse DCT- Parallel architectures for rank -order filters- Pipeline interleaving in digital filters- Pipelining in 1st-order and higher-order IIR Digital Filters- Parallel processing for IIR Filters- Combined pipelining and parallel processing for IIR Filters.

**Unit IV: Finite Word Length Effect in Pipelined Architecture**
9 Hours

**Unit V: Instructional Activities**
9 Hours
Design and simulate FIR and IIR filters for the given specifications study of finite word length effect in different realization
References Books:


Hyperlinks:

1. http://www.nptel.iitm.ac.in
2. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals

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<td>ADVANCED EMBEDDED SYSTEM</td>
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**Prerequisite:** Knowledge in embedded system

**Objective:** To provide the fundamentals on design attributes of functional units of a Processor and Hardware software partitioning in system design

**Outcome:** Understand the timing and interrupt in processor, the memories and communication protocol in embedded field and design a simple processor model

**Unit I: Introduction to Embedded Hardware and Software**  
9 Hours


**Unit II: System Modeling With Hardware/Software Partitioning**  
9 Hours


**Unit III: Hardware/Software Co-Synthesis**  
9 Hours

The Co-Synthesis Problem - State-Transition Graph - Refinement and Controller Generation - Distributed System Co-Synthesis.

**Unit IV: Memory And Interfacing**  
9 Hours


**Unit V: Instructional Activities**  
9 Hours

Design Process Model - Embedded System modeling with Hardware/Software Partitioning. Develop a model arbitration multilevel bus architecture and digital camera.
Reference Books:

Hyperlinks:
1. www.vectorindia.org/embedded_coursecontent.html
2. www.cetpainfotech.com
3. http://nptel.ac.in/courses/117106030/35

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<td>ADVANCED IMAGE PROCESSING</td>
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**Prerequisite**: Fundamentals of Signals and Systems

**Objective**: Make the students to understand the concepts used in image processing techniques and its analysis.

**Outcome**: Students will be able to work with various image processing techniques for real time applications.

**Unit I: Digital Image Fundamentals**  
9 Hours

Image fundamentals: Image acquisition - sampling and quantization - image resolution- basic relationship between pixels - color images - RGB, HSI and other models; Transform based models (DFT, DCT, DWT); Image Enhancement: Spatial and frequency averaging - smoothening and sharpening filters.

**Unit II: Segmentation and Denoising**  
9 Hours

Image Segmentation: Edge detection - edge linking via Hough transform - thresholding- region based segmentation; Denoising: Maximum likelihood estimation - Bayesian estimators - model selection (MDL principle) - transform based denoising - adaptive wiener filtering - soft shrinkage and hard thresholding.

**Unit III: Image Compression**  
9 Hours

Image compression: Basics of source coding theory (lossless and lossy) - Vector quantization - codebook design - transform and sub band coding.

**Unit IV: Image security and forensic**  
9 Hours

Image Security: cryptography and steganography techniques- Chaos based and Non-Chaos based methods; Image Forensics: Key photographic techniques-detection techniques for crime scene analysis.

**Unit V: Instructional Activities**  
9 Hours

Simulation of preprocessing techniques-implementation of image processing techniques for real time applications-forensic analysis using related tools.
Reference Books:

Hyperlinks:
1. www.imageprocessingplace.com/DIP-3E/dip3e_main_page.html

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<td>VEENG 632</td>
<td>CAD FOR VLSI CIRCUITS</td>
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Prerequisite: Basic knowledge in data structure algorithms

Objective: To Understand VLSI design automation tools

Outcome: Can understand Simulation and Logic Synthesis in VLSI design automation.

Unit I: Introduction to VLSI Design Flow 9 Hours
Introduction to VLSI Design methodologies: Basics of VLSI design automation tools-Algorithmic Graph Theory and Computational Complexity- Tractable and Intractable problems-General purpose methods for combinatorial optimization.

Unit II: Layout, Placement And Partitioning 9 Hours
Layout Compaction- Design rules- Problem formulation- Algorithms for constraint graph compaction- Placement and partitioning- Circuit representation- Placement algorithms-Partitioning.

Unit III: Floor Planning And Routing 9 Hours
Floor planning concepts: Shape functions and floor plan sizing- Types of local routing problems-Area routing- Channel routing- Global routing- Algorithms for global routing.

Unit IV: Simulation and Logic Synthesis 9 Hours
Simulation- Gate-level modeling and simulation-Switch-level modeling and simulation-Combinational Logic Synthesis- Binary Decision Diagrams- Two Level Logic Synthesis.

Unit V: Instructional Activities 9 Hours
Study of Hardware models for high level synthesis, internal representation- allocation- assignment and scheduling- scheduling algorithms- Assignment problem- High level transformations.
Reference Books:

Hyperlinks:
1. www.facweb.iitkgp.ernet.in/~isg/CAD/index.html
2. nptel.ac.in/courses/106106088/

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<td>VEENG 633</td>
<td>DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS</td>
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**Prerequisite:** Basics of semiconductor device operation and VLSI design.

**Objective:** To study analog integrated circuits features design and analysis methods of analog and mixed mode VLSI circuits.

**Outcome:** Students will be able to design efficient analog and mixed mode VLSI circuits.

**Unit I: Data Converters**  
9 Hours  
Data Converter Fundamentals: Analog versus digital discrete time signals - converting analog signals to data signals- sample and hold characteristics - DAC specifications - ADC specifications - mixed-signal layout issues.

**Unit II: Data Converter Architectures**  
9 Hours  
Data Converter Architectures: DAC architectures - digital input code - resistors string - R-2R ladder networks - current steering - charge scaling 0 DACs - cyclic DAC - pipeline DAC - ADC architectures – flash ADC - 2-step flash ADC - pipeline ADC - integrating ADC - successive approximation ADC.

**Unit III: SNR in Data Converters**  
9 Hours  
Data Converter SNR: Improving SNR using averaging (Excluding Jitter & averaging onwards) - decimating filters for ADCs (Excluding Decimating without Averaging onwards) - interpolating filters for DAC - band pass and high pass sync. filters.

**Unit IV: Operational Amplifiers and Mixed Signal Circuits**  
9 Hours  

**Unit V: Instructional Activities**  
9 Hours  
Design and simulation of different VLSI Circuits: Current mirrors - Differential Amplifier - PLL - ADC/DAC
Reference Books:

Hyperlinks:
1. http://nptel.ac.in/courses/117101105/
2. http://nptel.ac.in/courses/117101106/
3. http://nptel.ac.in/courses/117106034/
4. http://nptel.ac.in/courses/117106030/

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<tr>
<td>VEENG 634</td>
<td>DISTRIBUTED EMBEDDED COMPUTING</td>
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**Prerequisite:** Knowledge in Data Communication Networks and Microcontrollers

**Objective:** To provide knowledge in distributed embedded computing architecture

**Outcome:** Gain knowledge in distributed embedded computing architecture.

**Unit I: Internet Infrastructure**  
9 Hours


**Unit II: Internet Concepts**  
9 Hours

Capabilities and limitations of the internet - Interfacing Internet server applications to corporate databases HTML and XML Web page design through programming and the use of active components.

**Unit III: Embedded Java**  
9 Hours


**Unit IV: Embedded Agent**  
9 Hours

Introduction to the embedded agents - Embedded agent design criteria - Behaviour based, Functionality based embedded agents - Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

**Unit V: Instructional Activities**  
9 Hours

The product concepts- Automotive -Engine Control- Modeling the design of the Product Concept- Embedded System design and development life cycle model- Creating a basic VHDL for the entity of the memory block- Arithmetic and logic Unit.
References Books:


Hyperlinks:

3. www.pa.icar.cnr.it/cossentino/AOSETF10/docs/jamont.ppt

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<tr>
<td>VEENG 635</td>
<td>HARDWARE SOFTWARE CO-DESIGN</td>
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**Prerequisite:** Basic knowledge of testing techniques in Embedded System

**Objective:** To learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions.

**Outcome:** Gain knowledge in the fundamental building blocks of the hardware and software co-design and related implementation, testing environments, techniques and their inter-relationships

**Unit I: System Specification and Modeling**


**Unit II: Hardware/Software Partitioning**

The Hardware/Software Partitioning Problem - Hardware/Software Cost Estimation - Generation of the Partitioning Graph - Formulation of the HW/SW Partitioning Problem, Optimization - HW/SW Partitioning based on Heuristic Scheduling - HW/SW Partitioning based on Genetic Algorithms.

**Unit III: Hardware/Software Co-Synthesis**

The Co-Synthesis Problem - State-Transition Graph - Refinement and Controller Generation - Distributed System Co-Synthesis.

**Unit IV: Prototyping and Emulation**


**Unit V: Instructional Activities**

Design a System Level Synthesis - by learning the basics of the Xilinx Vivado High Level Synthesis (HLS) CAD Flow: Design Entry - Compiling and Simulation - Create a complete Hardware/Software Co-design that integrates the Arm Processor with an IP.
Reference Books:

Hyperlinks:
1. https://www.slideshare.net/destruck/hardware-software-codesign-16146924

VEENG 635
Prerequisite: Knowledge in design of electronic and microwave circuits

Objective: To familiarize the student with the technology and applications of Micro-Electro Mechanical Systems (MEMS).

Outcome: Students will be able to design different types of MEMS based devices, circuits and subsystems.

Unit I: Introduction to MEMS

Unit II: Micromachining Technology for MEMS
Fabrication Process: MEMS fabrication technologies - bulk micro machining - surface micro machining - LIGA process; Bonding and packing of MEMS - MEMS reliability - scaling in MEMS; Recent research direction in MEMS: CMOS- MEMS integration - polymer MEMS - NEMS etc.

Unit III: Sensor and Actuators

Unit IV: RF MEMS
Switches: Cantilever MEMS based switch; Inductors and Capacitors: Modeling and design issues of planar inductor and capacitors; RF Filters: Modeling of mechanical filters; Phase Shifters: Classifications and limitations; Micro Machined Antennas: Micro-strip antennas - design parameters.

Unit V: Instructional Activities
Modeling, simulation and analysis in the applications of MEMS switch, sensors and actuators using related platform.
Reference Books:

Hyperlinks:

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<td>VEENG 637</td>
<td>NANO ELECTRONICS</td>
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**Prerequisite**: Basic knowledge of electronic devices and its structures.

**Objective**: To introduce the characteristics and applications of nanoelectronic devices and its characteristics

**Outcome**: Familiar with certain nanoelectronic systems and building blocks such as: low-dimensional semiconductors, heterostructures, carbon nanotubes, quantum dots, nanowires etc.

**Unit I: Introduction**  
9 Hours  

**Unit II: Nanoscale CMOS**  
9 Hours  
Survey of modern electronics and trends towards nanoelectronics CMOS scaling, challenges and limits, static power, device variability, interconnect - CNT-FET, HEMT, pHEMT, FinFET, Ferro FET nanoscale CMOS circuit design and analysis

**Unit III: NanoElectronic Structure And Devices**  
9 Hours  

**Unit IV: NanoElectronic Memories**  
9 Hours  
Nanotube for memories - Nano-RAM - Nanoscale DRAM, SRAM, Tunnel magneto resistance- Giant magneto resistance- design and applications.

**Unit V: Instructional Activities**  
9 Hours  
Assignment and presentation on Nanolithography- Importance of micro/nanopatterning- Classification of lithographic techniques- Photolithography - A conventional and classical method - Ion beam Lithography - X-ray lithography - Electron beam lithography - Alternate Nanolithographic Techniques
Reference Books:

Hyperlinks:
1. onlinelibrary.wiley.com › Materials Science › Analysis/Characterization of nanosystems

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<tr>
<td>VEENG 638</td>
<td>PERVERSIVE DEVICES AND TECHNOLOGY</td>
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Prerequisite: Knowledge in Wireless networks and Mobile communication devices

Objective: To expose the fundamentals of pervasive computing and security in mobile computing

Outcome: Can design and deploy wireless sensor networks for specific applications

Unit I: Introduction
Ubiquitous or Pervasive Computing - Context - Definitions and types Context–aware Computing and Applications - Mobile computing-Networks- Middleware and gateways-Applications and services- Developing mobile computing applications- Architecture for mobile computing- Design considerations for mobile computing.

Unit II: Pervasive Networking

Unit III: Pervasive Devices
Introduction with Case study of - PDA - Mobile Phone: Elements - Mobile Information Architecture - Mobile Phone Design - Android Overview - The Stack - Android User Interface - Preferences, the File System, the Options Menu and Intents.

Unit IV: Wireless Devices and Security Issues In Mobile Computing

Unit V: Instructional Activities
Case study on Emerging Wireless Technologies, IEEE 802.20 Mobile Broadband Wireless Access
References Books:

Hyperlink:
2. http://www.nptel.iitm.ac.in/courses
3. https://www.isoc.org

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<td>VEENG 639</td>
<td>ROBOTICS AND AUTOMATION</td>
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**Prerequisite:** Basic knowledge in electrical machines, electronic devices and microcontroller

**Objective:** To educate on formulation of manipulator Jacobians and introduce path planning Techniques and to introduce robot control techniques and Robotic applications

**Outcome:** It will provide a comprehensive educational environment and enable students to gain expertise in next generation robotics and automation systems

**Unit I: Introduction**  
9 Hours
Definition-Classification-History - Robots components-Degrees of freedom-Robot joints-coordinates - Reference frames-workspace - actuators-sensors - Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors-proximity and range sensors-vision system-social issues

**Unit II: Robot Arm Kinematics**  
9 Hours
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

**Unit III: Robot Arm Dynamics**  
9 Hours
Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D’Alembert equations of motion

**Unit IV: Robot Applications**  
9 Hours
Material Transfer & Machine Loading / Unloading - General Consideration in robot material handling transfer applications – Machine loading and unloading.  
**Processing Operations:** Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

**Unit V: Instructional Activities**  
9 Hours
Design and develop robotic arm using ARM processor - Line follower models
Reference books:

Hyper Links:
1. http://www.nptel.iitm.ac.in

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<td>VEENG 640</td>
<td>SYSTEM- ON-CHIP DESIGN</td>
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**Prerequisite**: Basic knowledge in Processor Architecture

**Objective**: To learn System on chip fundamentals, their applications and to learn the various computation models of SOCs

**Outcome**: Students will be able to discuss System-on-chip fundamentals, their applications and On-chip networking methods.

**Unit I: Introduction**
9 Hours

**Unit II: Processors**
9 Hours

**Unit III: Memory Design For SOC**
9 Hours

**Unit IV: Interconnect Customization And Configuration**
9 Hours

**Unit V:Instructional Activities**
9 Hours
SOC Design approach: simulate and verify AES algorithms- design and evaluation of Image compression - JPEG compression.
References Books:
4. Jason Andrews and Newnes, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Bk and CD-ROM.

Hyperlinks:
1. http://ic.sjtu.edu
2. http://nptel.iitm.ac.in

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<td>VEENG 641</td>
<td>VLSI FOR WIRELESS COMMUNICATION</td>
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**Prerequisite**: Knowledge in Analog and Digital Communication

**Objective**: To study the design concepts of low noise amplifiers and to study the various types of mixers designed for wireless communication.

**Outcome**: Understanding of application of VLSI circuits in wireless communication.

**Unit I: Components and Devices**
9 Hours

**Unit II: Mixers**
9 Hours

**Unit III: Frequency Synthesizers**
9 Hours

**Unit IV: Sub Systems**
9 Hours
Data converters in communications, adaptive Filters, equalizers and transceivers.

**Unit V: Instructional Activities**
9 Hours
Simulation for different Mixer circuits and Frequency Synthesizers using the appropriate simulation tool.
Reference Books:

Hyperlinks:
1. http://nptel.iitm.ac.in

VEENG 641

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